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Application Note 30

Macro File Operation for Compression Load Pull Measurements

This note describes a measurement algorithm, which allows full load pull tests while automatically driving transistors into desired Compression Status and then measuring a selection of parameters, such as Output Power, Gain, Efficiency, Intermod, ACPR, DC Bias and Harmonic Loads. Examples of measured load pull contours and 3D surface plots are included.

Introduction

Load Pull measurements grew beyond standard Output Power, Gain, Efficiency or Intermod type of tests. Modern systems take measurements under sophisticated user defined test conditions. Those include "Constant Output Power", "Constant ACP", or "Constant Efficiency" type of measurements [1] or "MACRO File" [2] type of tests.
Another type of test, often required by test engineers, is measurement of a selection of test parameters under "Gain Compression" conditions.
The CCMT test software has been enhanced to make this test using its MACRO File measurement capability [2].
The test is controlled by a Measurement Macro File, which includes all parameters to be measured after the DUT has reached the desired gain compression status.
An interpolation and extrapolation formula allows to fine tune the source power to the closest saturation point within the source power range.
Load Impedances for which compression status cannot be reached are marked on the Smith Chart. Gain Expansion is also measured and saved in the load pull file as an independent parameter.
This note describes the setup, procedure required to run such tests and limitations to be expected. It also presents some sample results in form file listings, ISO contours and 3D plots.

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System Description and Definitions

The CCMT (Computer Controlled Microwave Tuner) load pull system includes two programmable tuners (model 1808, operating from 0.8 to 18 GHz), an IBM-PC compatible tuner controller, GPIB interface, calibration and measurement software (figure 1). The tuners and the other passive components of the setup, including test fixture, are calibrated beforehand on a vector network analyzer. The network analyzer must be calibrated using coaxial TRL for adequate accuracy. The load pull software allows for TRL calibration of the transistor test fixture and de-embedding of all measured data to the DUT reference plane. The overall accuracy of the calibrated system is verified using the "back-to-back" method, in which a Thru line is inserted in the test fixture and the tuners are driven to conjugate complex impedances. The total gain is then measured close to 0 dB. The system is calibrated at 181 or 361 discrete points on the Smith Chart, up to reflection factors of 0.9 and can be used without re-calibration for several months. The control software allows to synthesize any interpolated impedance with an accuracy of better than 40dB, within the tuning range. The resolution thus obtained exceeds 10,000,000 impedances at 1 GHz. Fine tuning is possible using the computer cursors, the mouse or a keyboard entry. Parasitic oscillations are practically eliminated because the tuners, having a low pass behavior, present to the transistors roughly 50W at all frequencies below 800 MHz.

In addition to impedance tuning, the load pull software includes some other unique features, such as automatic search for maximum gain, output power and efficiency. This search does not involve load pull but a direct gradient search with fine tuning resolution. For the purpose of this work a new algorithm has been developed which allows peak search of output power or gain under gain compression conditions. This means that for each tuned impedance during the gradient search, the input power is swept until the transistor reaches the desired compression level. The power or gain are then measured and compared with the previously measured values to determine the direction of the next step in the search. Despite its complexity, this routine takes only a few minutes to converge and delivers, especially in source pull, very useful data, which cannot be obtained easily, except by using alternate and lengthy compression source and load pull tests.

The Macro file operation drives the complete measurement setup from a script (ascii) file, which can be generated either from inside the load pull system or by using a simple editor program (such as EDIT or NOTEPAD).

A multitude of macro commands allow for simple, medium and very complex operations [1]. Simple macro commands include keywords like INIT (for tuner initialization), TUNE (for impedance synthesis), GPIB for direct GPIB control, and more complex ones, such as BIAS (for controlling the DC bias of transistors), PIN_POUT (for saturation measurements), PEAK (for automatic search of maximums) and C_PEAK (for searching maximums under compression conditions).

The most complex macro commands include LOAD_PULL (for complete load pull with Pin=constant), COMPR_LP (for complete load pull at Pin levels up to X-dB of compression in which all RF parameters are saved during the Pin sweep) and REG_LP (for constant Pout or Drain current load pull). The "Design Window" evaluation software presented in this work makes use of the measurement data obtained during the execution of the "COMPR_LP" macro command.

An important feature includes FIND_OPT, which allows to tune the tuners to the optimum point found during the latest measured load pull file for any specific measured parameter, such as Intermodulation or ACP, Efficiency, Gain etc. A completely automatic operation without time or memory limitations is possible especially since the macro vocabulary includes the keyword FILE, which allows to execute other macro files (=subroutines). For a complete list of macro commands see [1].

Compression Load Pull

The Macro file operation not only includes a set of commands the system executes sequentially but also a list of parameters that are measured and saved in sequence. If the first parameter in the list is the token GCOMPR (for Gain COMPRession), then, for each tuned impedance, the input power will be swept to reach the desired compression status (e.g. X dB) relative to a gain reference level. This level can be defined either as the small-signal gain or the peak gain in a gain expansion characteristic. The last step of the power sweep is interpolated in order to obtain as close a compression to the target value as possible. Once this is done the list of parameters following in the Macro File is measured and saved. In other words, all values are measured under X-dB compression conditions. The Contour Graphics program then processes the data to ISO contours of any combination of two of the measured parameter values as shown in figures 2, 3. Figure 2 shows load pull power contours of a Silicon bipolar transistor at 1 GHz. The round contours correspond to a low and constant input power, whereas the elliptic contours are the 1dB compression power contours. The significant effect of saturation can be observed. Figure 3 shows an overlap of Adjacent Channel Power (Sideband 1) and 1dB compression power of another transistor (HBT) at 836 MHz. The ACP and P1dB maxima are almost 180 degrees apart and compression load pull is obviously the only way to identify an acceptable compromise.

Design Window Load Pull

The Design Window Load Pull algorithm consists of four steps:

1. Move the tuner to a load (source) impedance
2. Sweep the Input Power from Pin,min to Pin,X-dB.
3. Measure and Save the selected set of RF parameters for each input power (use "COMPR_LP" macro).
4. Interpolate the last power step to get close to X-dB compression. Record this final set of data.

The selected set of parameters to be measured may include any of the following items: Pin, Pout, Gain, Efficiency, IMD, ACP (average of each channel or individually all four upper and lower side bands), DC Power, Input and Output Currents and Voltages and Harmonic Impedances.

When the load pull routine has gone through all tuner points, which normally cover the complete Smith Chart (or part of it according to a user defined pattern), the data file can be processed by an evaluation program. This program first displays the list of the measured parameters with their minimum and maximum values and allows to define a set of targets for all or part of the parameters. Such a target can, for example, be ACP-1 > 46 dBc. Once this is done, the data file is scanned for the impedance points and input power conditions at which all target values are simultaneously satisfied and saves those data points in a "Design Window" file. These points can be displayed on the Smith Chart together with the associated target values and can be modified "on-line" through the CCMT control software. Figure 4 shows such a "Design Window" example for the HBTs operating at 836MHz, whose compression contours were illustrated earlier (figure 3).

Importance of this Test for Design Engineers

The Design Window evaluation technique is very important for designs of amplifiers which involve several design targets simultaneously, such as Gain, Pout, Efficiency, ACP and DC currents.

In general, the load lines for output power, efficiency and ACP are functions of the input power as well as the test conditions under which they were measured. For example, the Gain and Output Power contours coincide when the L/P measurement is performed under a constant Input Power level (conventional Load-Pull measurement) but are located in different areas of the Smith Chart when the L/P measurement is carried out under compression conditions or constant Output power conditions. The interpretation of Load-Pull measurements obtained under such conditions can assist the determination of circuit design conditions that, in the best case, meet only limited part of the specs. For example, the compression load pull contours can lead to the determination of conditions that lead to maximum saturated Output Power or Efficiency or ACP but not an optimum combination of the latter parameters. Since the ACP and Gain behavior are different than those of the Efficiency, the load pull data also must be considered for a variety of input powers, since the best compromise for those quantities may not necessarily be at PX-dB. input power level. Finally, conventional L/P measurements are very difficult to correlate to realistic amplifier specs since they are performed under constant input power levels and will not reveal the areas on the Smith Chart where device linearity is best.

It is thus very time consuming to search through the large amount of data produced by a conventional load pull system for an optimum solution combining most or all of those design criteria. Design Window makes this search very efficient. The complete data are available at any time and even when modified specifications are issued, the designer has only to recall the data and apply the new target specs in order to determine a new design window i.e. all source and load impedance conditions meeting amplifier specs. Design Window is a powerful technique which allows almost "on-line" negotiations on specifications with customers. This gives a leading edge to any supplier of sophisticated amplifiers, especially in the cellular and PCS band, where cost is a prime consideration but linearity and efficiency cannot be compromised.

Adjacent Channel Power Measurement Routine

The CCMT load pull software is capable of accurately measuring ACP ratio since 1993. It supports all available spectrum analyzers from Hewlett-Packard, Anritsu, Advantest and Rohde&Schwarz. It uses both AUTO option (for spectrum analyzers equipped with this feature) and CUSTOM, for user defined tests [2]. The results presented here use a recent upgrade of this software, which allows a more accurate determination of Signal Power included in the CDMA channel. This power can be determined over the entire (user defined) bandwidth of the CDMA channel (typically 1.23 or 1.25 MHz). The two sidebands (typically at +/-885 kHz and +/-1.98 MHz off center frequency) can also be set by the user. The new routine allows also for simultaneous or individual registration of power leakage into each of the sidebands and corresponding graphical processing of the measured load pull data into individual contours. A tradeoff between accuracy and speed is also possible since the user can determine the number of samples he wishes the routine to take inside the CDMA channel in order to determine the power. The routine has been applied on spectrum analyzers which include the AUTO option as well and found to produce identical results. In other words any older spectrum analyzer can be used to carry through those measurements with state of the art accuracy.

Measurement Examples

We measured a number of AlGaAs/GaAs Heterojunction Bipolar Transistors (HBTs), which can be used in Cellular and PCS applications. All tests were carried out at a collector-emitter voltage of 3V, Class-AB bias operating conditions and employed a CDMA excitation at 836 MHz. Prior to the design window compression load pull measurements, the source termination was optimized by means of the peak search routines that are available. Nonlinear modeling of the HBT behavior was also carried out and confirmed the accuracy of the measurement data and the device models.

The following plots and data listings show how the compression load pull and design window routines worked for the HBTs tested in this work. Figure 4 shows the on-line operation of the design window utility: The user can increase or decrease the displayed target values pressing the associated F-keys F1..F7 or Shift-F1 to Shift-F7. Then he can, on-line, scan through the complete data file by pressing F10 and plot all valid points in the Smith Chart. Then he/she can very easily either identify the points which satisfy all target conditions given by the specifications or alternatively, move all targets, one by one, to their highest acceptable limit for the number of valid impedance points required. In this particular example only three impedance points are satisfying all target values at once. The target values include: Pout, Efficiency, Gain, ACP-1 and ACP2 and Input and Output DC current. The design window shown on figure 4 represents the optimum tradeoff, at the load plane, between the measured RF parameters at the particular bias, frequency, source termination conditions, according to the pre-determined power amplifier specifications.

The data listing in table 1 shows the contents of the Design Window of Figure 4. The data show that all conditions may be fulfilled at each load impedance point for more than one level of input power and that the conditions are not necessarily fulfilled at all points for the same input power. This confirms the claim earlier that a power sweep is necessary in order to identify the optimum conditions in of multi-parameter load pull data file. In other words load pull tests based on a single input power level are not adequate to identify the optimum conditions of a multi-parameter test. The parameter æPtÆ signifies which load impedance point has been tuned to (out of 361 calibrated points). The target values to be fulfilled simultaneously in order to generate the Design Window file (.DWN) below are: Pout > 20.4dBm, Gain > 19.5dB, Efficiency > 35.0%, ACP-1 > 46.2 dBc, ACP-2 > 55 dBc, Base Current < 0.1 A and Collector Current < 1.0 A.

```
! DESIGN WINDOW DATA FILE =C:\CCMT\DATA\TEST.DWN
! ==============================================
! data from following .LPC file:
! Load Pull Measurement Data
!----------------------------------
! File = C:\CCMT\DATA\TEST.LPC
! Date = Thu Jun 05 18:39:18 1997
!----------------------------------------------------
! Comment = Measured from Macro File..
! Frequency = 0.8360 GHz
! Char.Impedances = Source: 50.00 W, Load: 50.00 W
! Source Impedance = 9.68 +j 13.38 W
!----------------------------------------------------
Pt    R[W]   X[W]   PIN      POUT    GAIN     EFF      ACP-1   ACP-2    I-INP   I-OUT

!--------------------------------------------------------------------------------------------------
074  16.75  -3.48   -1.209    20.626   21.835   36.445   47.415   58.080    0.002    0.106
075  16.39  -9.86   -0.149    20.683   20.832   38.241   46.334   59.595    0.002    0.101
099  11.81  -5.83    0.841    21.535   20.695   35.226   47.195   58.793    0.003    0.133
```

Table 1: Content of Design Window File of figure 4.

Visualize Transistor Behavior using 3D Plots

The 3D surface plot capability of the CCMT graphics is useful for visualizing the qualitative behavior of transistors in load pull tests. The surfaces generated identify immediately any oscillations or other anomalies and also help understand better the 2D contour plots. Due to mathematical smoothing used in all 2D contouring algorithms particular characteristics of the device behavior may be lost, especially because some people prefer to see smooth contours, which rather correspond to their expectations. 3D surfacing of the CCMT software does not smooth out any point. It shows the reality as is. Figure 5 shows the general behavior of ACP sideband 2 over load impedance at 1dB gain compression for the tested HBT at 836 MHz. We observe, as a matter of fact, two areas of high ACP-2: one close to the maximum power at very low impedances and one opposite to it at high inductive loads.

Finally, figure 6 presents (for the first time) the general behavior of Gain Expansion of an HBT . Gain Expansion being defined as Gmax - Gmin during the input power sweep at every load impedance. Gain expansion is a significant indication for linearity of the device and it also identifies the area of the Smith Chart where the load conditions drive the device into class "C" type of operation (Gain Expansion is typical for class "C" operation).

Conclusion

A compression load pull measurement and design window evaluation routine has been presented. It allows fast knowledge on the capacity of DUTs to fulfill target specifications in a realistic large signal operation environment. Results have been presented for combined conditions such as Pout > Target 1, ACP > Target 2, Efficiency > Target 3, I-base < Target 4 and I-collector < Target 5, all target values being User defined. The software enables, for the first time, the unique determination of the tradeoffs between Output Power, Efficiency and ACP for a particular transistor at all load impedances and input power levels allowed.

Measurement Setup

The following setup can be used to measure all three types of Efficiency. Depending on the case Power Meter 1 (C-Eff) may not be required. Power meter 3 is only used here for demonstration purpose in order to explain the relation between the different powers flowing through the setup.

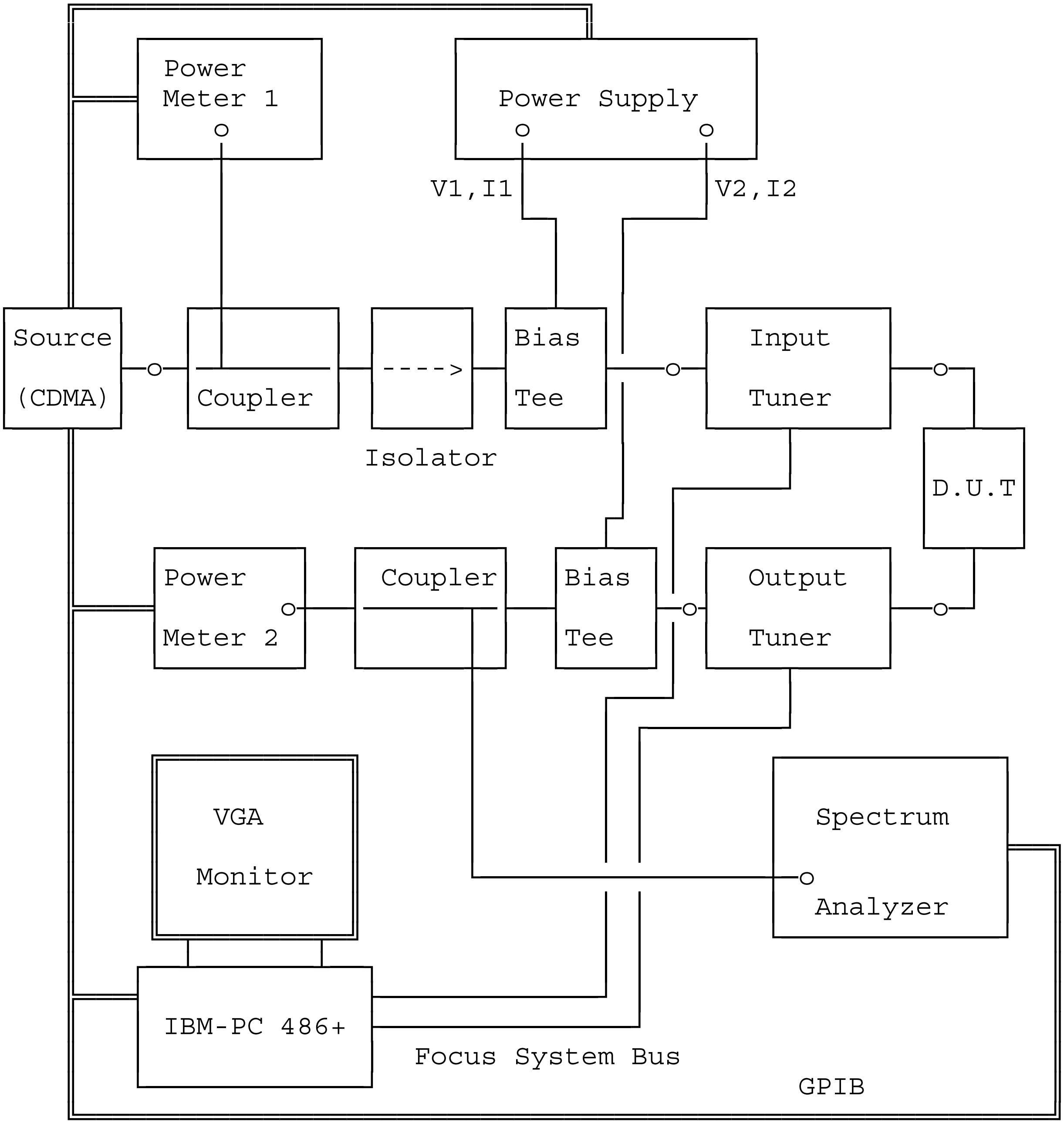

Figure 2: Load Pull Setup for measuring Gain, Power, Efficiency and ACPR.

References

[1] "CCMT Manual", Section 4, Load Pull Measurements, Focus Microwaves

[2] "MACRO File Operation of CCMT Software", Appl. Note 28, Focus Microwaves, 1996