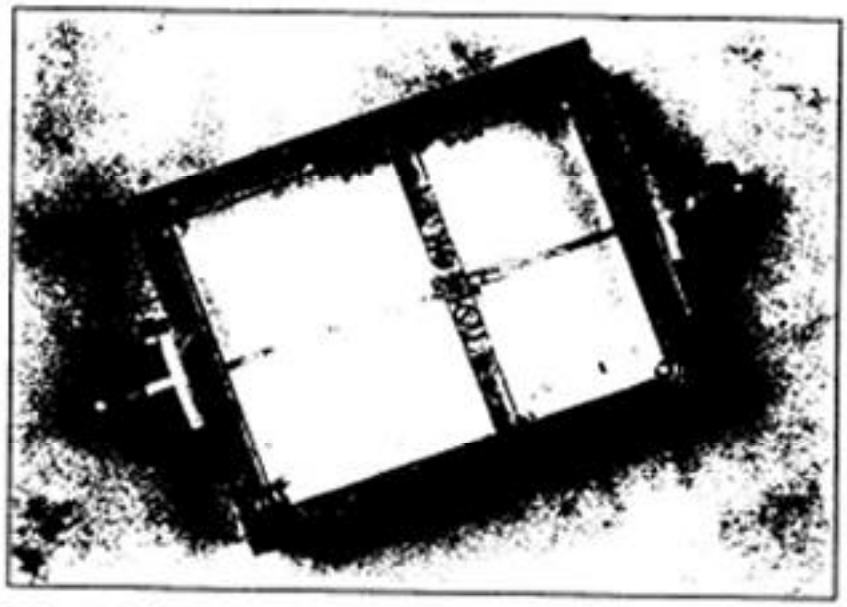
FOCUS Microwaves inc.

TECHNICAL NOTE 1-92

•MEASUREMENT •DESIGN and •TEST Tools

Design A Power Amplifier Stage Using μW-PADS



3.7 – 4.2 GHz Power Amplifier, version 1.

Courtesy France Telecom, CNET-Paris B, ST/SH/VP

SUMMARY

The Microwave Power Amplifier Design Software (μW-PADS) permits the design of amplifier stages practically up to saturation level using only measured power contour data. This note describes the procedure used to:

A. Characterize a power FET using the programmable tuner system.
B. Transfer power contour data to μW-PADS and design the amplifier.
C. Verify the design's performance using the tuners.
D. Manufacture, test and compare the amplifier's performance to the designed values.

The measured power and gain of the first iteration 3.7 – 4.2 GHz MIC amplifier agree within ±0.1dB with the designed values without any adjustment.

A. Characterize the power FET using the Computer Controlled Microwave Tuner (CCMT) System

The CCMT system permits full power characterization of FETS. The setup used is shown in figure 1. After tuner calibration on a Network Analyzer, the other setup components of figure 1 are also characterized using the SETUP utility of the CCMT software. This includes all twoports in the setup and very particularly a TRL capability for the test fixture. The small signal 'S' parameters of the FET are also measured and saved in an ASCII file in Touchstone™ compatible .S2P format. After all these data are saved on files the system can operate independently on the Network Analyzer.

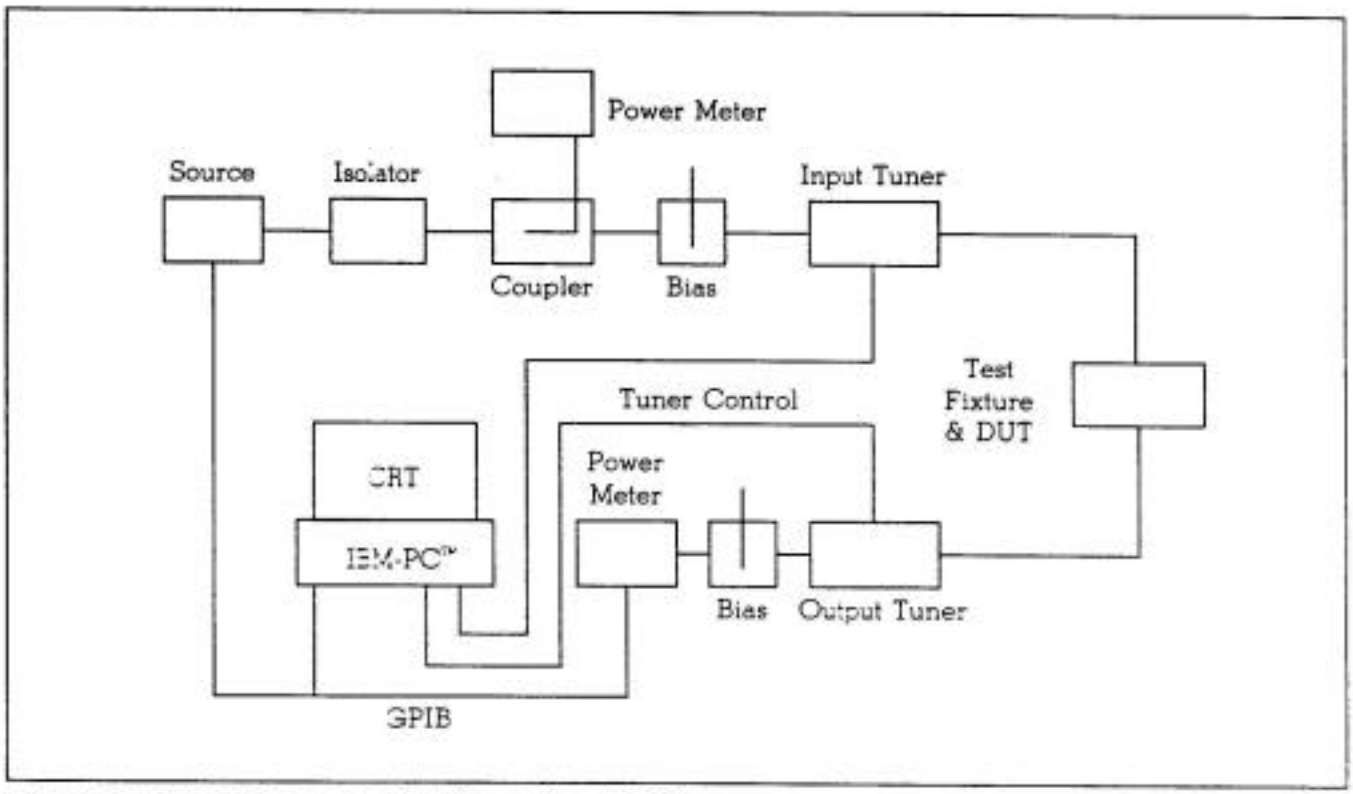


Figure 1 Automatic Load Pull Setup for PADS.

The PADS routine of the CCMT Power menu characterizes the FET systematically in the required frequency range. It executes fully automatically the following operations:

1. Step through the frequency range
2. Load tuner and setup data
3. Deembed to FET reference plane
4. Tune output tuner to pre-match the output
5. Tune to match the input
6. Transfer the input tuner's conjugate complex reflection factor Γ_s^* to the FET's .S2P file and replace S11. The new file carries the same name but the extension .L2P (L for Large signal matching).
7. Fine tune to match the output (in order to compensate for second order effects due to S12 > 0)

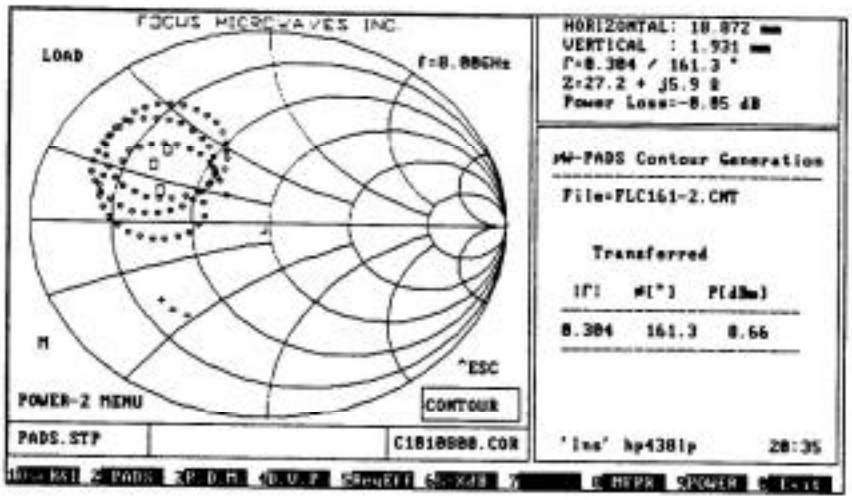


Figure 2

8. Tune the output tuner to a circle around the maximum point, measure output power, corrected to the FET output terminals, and transfer the data to a contour data file (extension .CNT) Figure 2 shows the typical operation screen of the CCMT software during operation of the PADS routine.

B. Use μW-PADS to design the power amplifier stage

The μW-Power Amplifier Design Software package needs the following data in order to operate:

B1. A power contour data file (.CNT)
B2. An .L2P (or .S2P) S-parameter data file.
B3. A Touchstone™ compatible circuit file (.CKT), describing in nodal form the input and output networks of the amplifier.

B1. An extract of a power contour data file (.CNT) is given in figure 3. It includes some comment on the FET tested and test conditions and for each frequency the following information:

1. Reflection factor for and value of maximum output power.
2. Reflection factor on the circle around the maximum and the associated measured power.

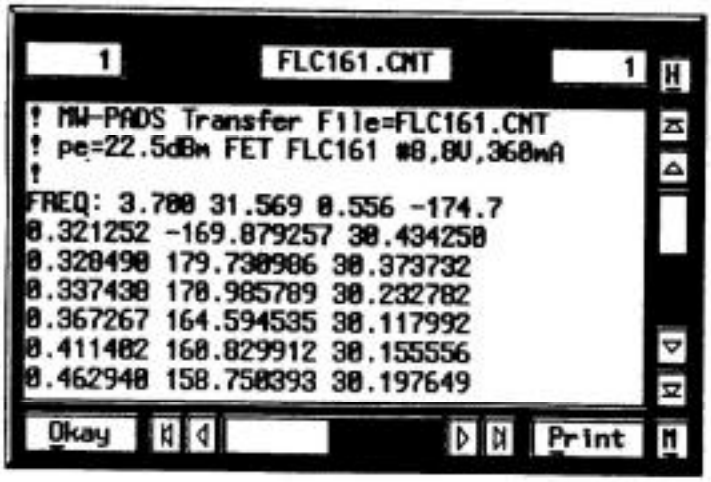


Figure 3

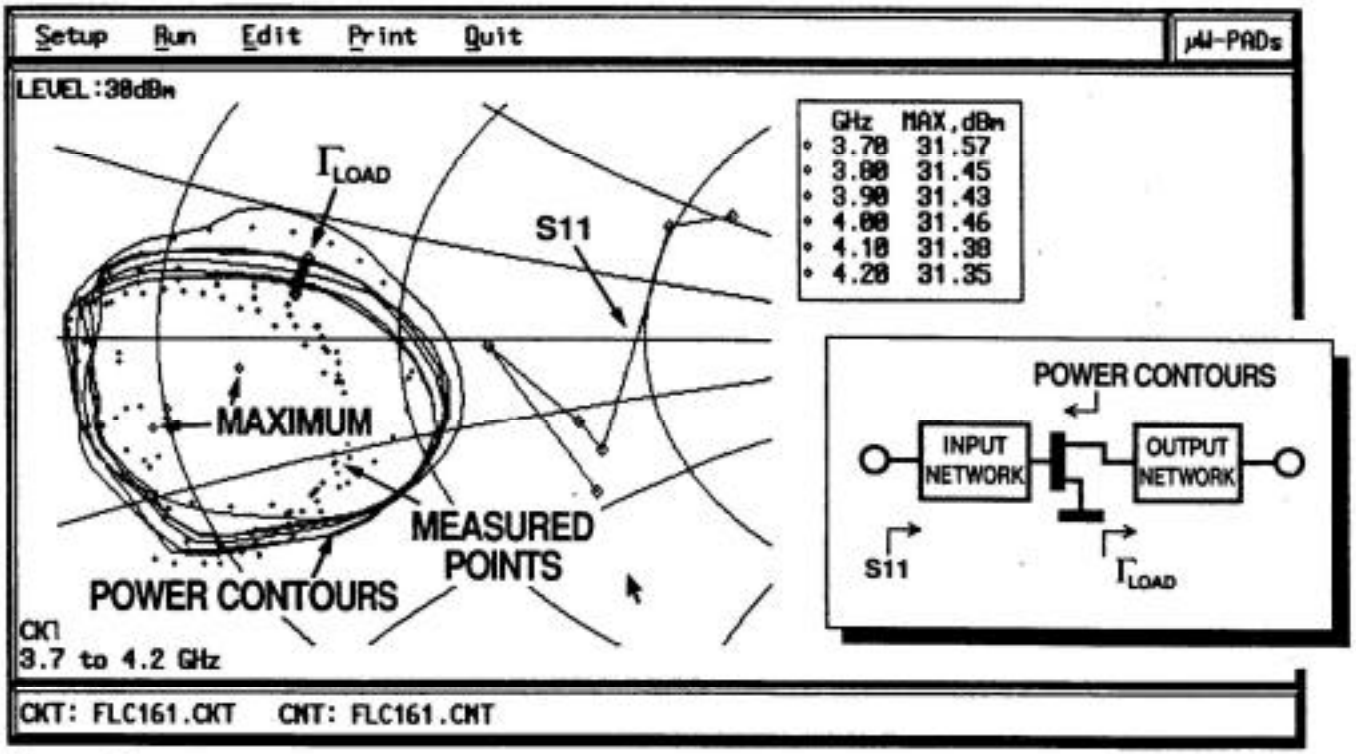


Figure 4

This file can be retrieved automatically by μW-PADS which can then generate ISO power contours for network optimization.

Once the data are retrieved the measured contour points are shown on the screen in order to make the network design process easier for the user of the system. μW-PADS includes a 2nd order interpolation utility that permits the generation of ISO power contours at any power level up to saturation, using data from one set of measurements (.CNT file) only.

In order to facilitate the operation the user can request the software to generate ISO power contours at a power level close to his requirement. Fig 4 shows the measured points and associated power contours at 30 dBm constant power.

B2. Examples of .S2P and modified .L2P data files that include large signal input matching information for the FET are shown in figure 5. The large signal input reflection of the FET is used for designing the input network at actual injected power level.

B3. The network description file (extension .CKT) uses familiar format (Touchstone™) and can include most commonly used microstrip distributed and lumped elements, such as MTRL, MTEE, MSTEP,

Example of .S2P data file

```
! S-Parameter: FLC161Wf Vds=10V,Id=360mA
 Freq      S11          S21          S12
 3.700  0.862 157.5  1.655 43.9   0.041...
 3.800  0.862 156.2  1.600 24.3   0.039...
 3.900  0.862 154.8  1.544 7.2    0.038...
 4.000  0.863 153.5  1.489 -3.2   0.035...
 4.100  0.864 152.2  1.455 -10.5  0.034...
 4.200  0.864 150.9  1.422 -25.3  0.028...
```

Example of .L2P data file

```
! Large Signal data
Freq      S11          S21
3.700  0.820 163.2  1.655 43.9...
3.800  0.817 158.6  1.600 24.3...
3.900  0.810 164.0  1.544 7.2 ...
4.000  0.816 166.7  1.489 -3.2...
4.100  0.802 159.2  1.455 -10.5..
4.200  0.811 159.9  1.422 -25.3..
```

Figure 5

MOPEN, MSHORT, R, L, C, etc. Parts of such a network description file and optimization target definition are shown in figure 6.

The FET's small or large signal parameters can be included in the network description as twoports in .S2P format ASCII files. The software provides for interpolation between frequency points of .S2P or .L2P files and also power contour files (.CNT).

Optimization is possible using random, gradient or simplex optimizers, which are very efficient. Total network reflection factor and output power can be optimized to be less (LT) equal (EQ) or greater (GT) than target values set by the user. During optimization the user can observe

- the projection of the network's reflection factors into the power contours and the total network S11 (fig 4)
- the output power, referred to the network output and the magnitude of the input reflection factor (fig 7).

This way he can get a quantitative feeling of the obtained performance (fig 7), as well as exact information about the behaviour of the networks over the entire frequency range (fig 4). So modification to the network is possible by adding or changing microstrip elements, if the obtained performance is not satisfactory.

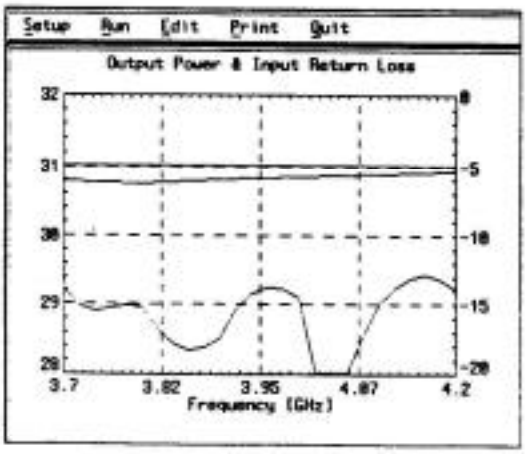


Figure 7

```
WI3=? 500 1569.15 1600 ?
LI3=? 500 3002.95 8000 ?
WI4=? 200 1451.26 1500 ?
LI4=? 680 732.267 6500 ?
 !
 ! Define 'S' parameter
 !---------------------
  files
  fic161.12p fet1
 !
 ! Define In Out networks
 !-------------------------
 ckt
MSUB ER=9.8 H=635 T=4 RHO=1 TAND=0.001
MTRL 1 2 W=W0 L=L0
MOPEN 3 0 W=WS L=LS
MOPEN 3 0 W=WS L=LS
MTRL 4 5 W=W2 L=L2
MTEE 2 4 3 W1=W0 L1=0 W2=W3 L2=0 W3=WS L3=0
MTEE 4 2 3 W1=W2 L1=0 W2=W0 L2=0 W3=WS L3=0
MTRL 6 7 W=640 L=2000
MSTEP 5 6 W1=W2 W2=640
DEF2P 1 7 OUTPUT
 .
 ! Define total network
 !-----------------------
INPUT 1 2 0
FET1 2 3 0
OUTPUT 3 4 0
DEF2P 1 4 NETW
 !
FREQ
SWEEP 3.7 4.2 .1
 !
 ! Define outputs
 !----------------
OUT
! INPUT S22
NETW S11
OUTPUT POWER
 !
 ! Define optimization targets
 !--------------------------
OPT
NETW S11 LT -14 W=1
OUTPUT POWER EQ 31 W=10
 !
 ! Define grid
 ! -----------
GRID
POWER 25 32 1
REFL -20 0
```

Figure 6

C. Design Verification

The CCMT system offers the possibility to verify the expected performance of the just designed amplifier by measurement in the same load pull setup, used for power contour generation, under the same test fixturing, bias and input power conditions. This is accomplished using the DVP (Design Verification Package) which is included in the CCMT operation software. In order to operate DVP the CCMT system requires

C1. Tuner calibration data in the frequency range of interest
C2. Measurement setup data
C3. S-parameter data for the input and output networks of the amplifier

The tuner calibration and setup data are the same used before for power contour generation. The network S-parameter are included in a .CKI (Input) and .CKO (Output) data file in .S2P ASCII format (fig 8). This data can be generated fully automatically by μW-PADS using the 'Save S-Par' utility in the 'Run' menu. S-parameter files, generated by Touchstone™ or other linear or nonlinear network simulators can also be used in DVP.

```
! CKT-FILE: FLC161.CKT
! NETWORK:  OUTPUT
! CNT-FILE: FLC161.CNT
! CONTOUR-LEVEL: 31.00dBm
!FREQ        S11             S12             S21             S22             POWER
!          MAG    ANG      MAG    ANG      MAG    ANG      MAG    ANG
  3.70   0.542 -152.2   0.835 -127.7   0.835 -127.7   0.538  76.6   30.78
  3.80   0.547 -153.0   0.832 -131.1   0.832 -131.1   0.542  70.6   30.75
  3.90   0.550 -153.7   0.830 -134.6   0.830 -134.6   0.545  64.4   30.80
  4.00   0.554 -154.3   0.827 -138.0   0.827 -138.0   0.549  58.2   30.85
  4.10   0.558 -154.9   0.824 -141.5   0.824 -141.5   0.553  51.8   30.89
  4.20   0.562 -155.4   0.822 -145.0   0.822 -145.0   0.556  45.3   30.91
```

Figure 8

The Design Verification procedure runs fully automatically and consists of

1. Stepping through the frequency range
2. Loading tuner calibration and setup data from disk into memory
3. Deembedding to FET terminal level
4. Measuring the power delivered from the system to the power detector
5. Replacing the tuner's and fixture's loss by the computed network's loss (from .CKI/.CKO S-parameters) and calculating the network's output power and gain.
6. Saving the test impedance and power/gain data on an ASCII file with the extension .VRF (for Verify).

The cartesian plot utility of the CCMT software then permits to plot the Design Verification against calculated power over the specified frequency range (fig 9).

A plot for the specific 3.7 - 4.2 GHz power amplifier stage is shown in fig 9. It shows a deviation of 0.1 to 0.2 dB at 31 dBm output power between **design** and **design verification.** This power corresponds to over 2dB gain compression (fig 10).

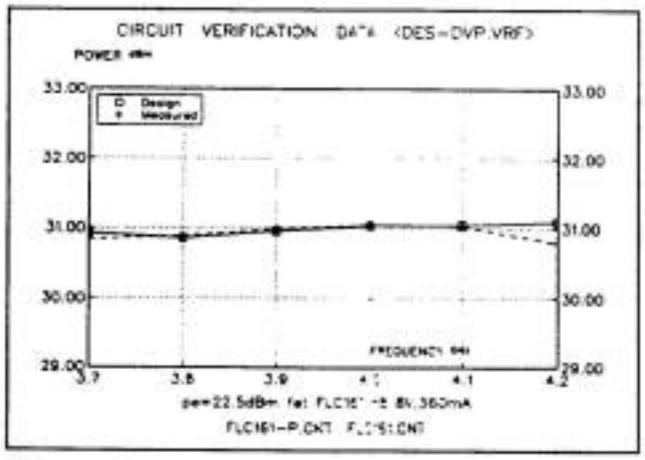


Figure 9

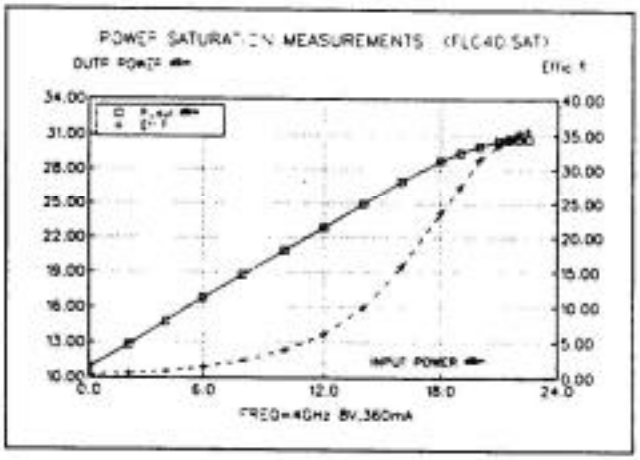


Figure 10

D. Manufacture and Test of the Amplifier

Two versions of the amplifier circuit have been designed and manufactured on 25mil thin film Alumina substate. Rubylith generation and conventional etching and assembly techniques could be used due to the absence of critical dimensions in the design. The final circuits have been mounted in test cases with SMA connectors and DC bias supply bypass capacitors (cover picture and fig 11).

The finished power amplifier stages have been tested in the same load pull setup, using the same components and instruments, except the test fixture and the tuners, in order to be sure there are no calibration errors in the measurement.

The performance of both maquettes is practically identical and shown in figure 12, compared to the design and verification values over the frequency range.

They show that the obtained output power performance of this amplifier stage is within ± 0.1dB of the designed value and within 0.15dB of the design verification value over the entire 3.7 - 4.2 GHz frequency range.

The same performance is obviously valid for the overall gain, since all the tests and the design are based on the same input power of 22.5dBm (Gain = 8.3 ± 0.1dB). The input return loss varies between 8 and 11dB at small signal and 7 and 9.5dB at large signal.

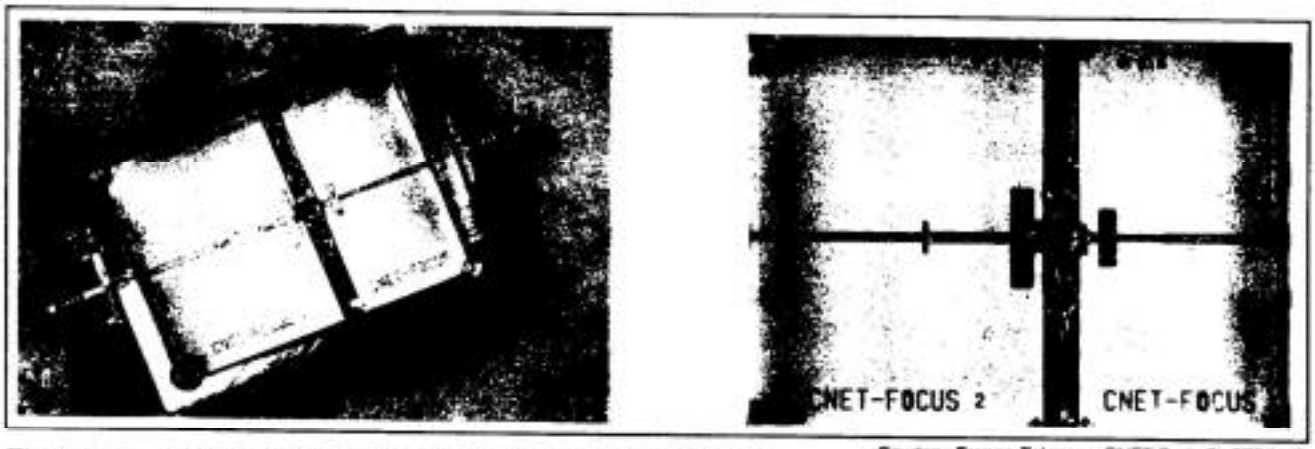


Figure 11 3.7 - 4.2 GHz Power Amplifier, version 2.

Courtesy France Telecom, CNET-Paris B, STS/HYP

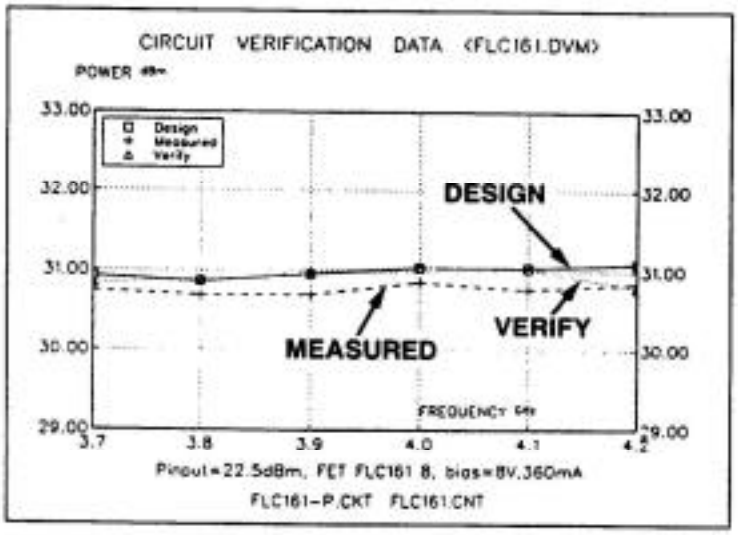


Figure 12

Conclusion

The programmable tuner system (CCMT) and the wideband power amplifier design software (μW-PADS) of Focus Microwaves have been used to characterize a power FET (FLC 161 WF of Fujitsu), design a 3.7 – 4.2 GHz power amplifier stage and verify this design. The realized amplifier provides 31dBm output power within ±0.1dB of the designed value, constant over the frequency range.

Performance of 3.7 - 4.2 GHz Power Amplifier
FET FLC161WF (Fujitsu) Bias 8V 360 mA
Input power 22.5dBm, Saturated.

GHz	Output Power dBm		Deviation dB	Gain dB		Efficiency %	IMD* dBc	Return Loss dB
	Design	Measure		Design	Measure			
3.7	30.93	30.83	**0.1**	8.43	8.33	36.8	-16.5	7.2
3.8	30.86	30.83	**0.03**	8.36	8.33	38.0	-15.3	7.7
3.9	30.96	30.81	**0.15**	8.46	8.31	38.9	-17.0	8.4
4.0	31.04	30.84	**0.2**	8.54	8.34	38.2	-16.5	9.2
4.1	31.04	30.87	**0.17**	8.54	8.37	38.2	-17.8	8.8
4.2	31.09	30.94	**0.15**	8.59	8.44	39.7	-16.0	7.8

*at total input power = 22.5dBm

Table 1

Table 1 shows the accuracy of the design method and the overall performance of the prototype amplifier. It is important to realize that these data result from a single iteration without any tweeking or circuit adjustment.

Outlook

μW-PADS has been extended and can operate with efficiency and intermod contours instead of power. Related results will be published in a future Technical Note.

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