Sub-0.2 dB Noise Figure Wideband Room-Temperature CMOS LNA With Non-50 Ω Signal-Source Impedance

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***Abstract*—This paper presents a wideband low-noise amplifier (LNA) designed to be used as the first stage of the receiver in the Square Kilometer Array radio telescope. The LNA design procedure and its layout features are discussed. The noise figure optimization procedure determines the signal-source resistance that results in reduced noise figure. When used in the radio telescope, the required signal-source resistance will be presented by the telescope custom-made antenna elements. The LNA, designed in 90 nm bulk CMOS, achieves sub-0.2 dB noise figure from 800 MHz to 1400 MHz, return loss of more than 11 dB, gain (S_{21}) of more than 17 dB driven into a 50 Ω load, output 1 dB compression point of 2 dBm, output IP3 of 12 dBm, and output IP2 of 22 dBm while consuming 43 mA from a 1 V supply. In the LNA implementation presented in this paper the load choke inductor and the source inductor are integrated whereas the gate-, bias-, and the choke-inductor between two transistors of the cascode are external. The noise figure of the presented LNA is to our knowledge the lowest noise figure achieved by a power matched wideband CMOS LNA at room temperature.**

***Index Terms*—CMOS, low-noise amplifier (LNA), noise measurement, noise optimization, radio astronomy, signal-source impedance, square kilometer array (SKA).**

I. Introduction

THE next-generation international Square Kilometer Array (SKA) radio synthesis telescope will require millions of receivers according to some estimates [1], [2]. The large number of very low-noise receivers puts pressure on the receiver cost. CMOS technology is the least expensive technology relative to exotic InP and GaAs technologies due to large manufacturing volumes. The constant improvement in CMOS transistors due to rapid scaling of their feature sizes is making the latest CMOS transistors capable of achieving noise figures low enough to be considered for radio astronomy [3].

The flexibility to select a nonstandard port impedance is available in the design of an SKA low-noise amplifier (LNA), as the telescope requires custom made antennas that can be designed with higher than 50 Ω port impedance [4]. In CMOS, it has been shown theoretically, with a simplified transistor model in [5], [6] that one can expect noise figure improvements in narrowband LNAs by increasing the signal-source impedance. A similar idea was previously tried experimentally for wideband LNAs with GaAs transistors in [4] and [7]. The authors in [8] discussed measurements of a non-50 Ω impedance CMOS LNA for the situation when power match is not required.

sIn this paper we show that the sub-0.35 dB noise figures that we achieved in [3] can be improved further by designing an LNA for the telescope antenna with non-50 Ω port impedance and using a power constrained optimization as described in [5] rather than the bandwidth and power constrained optimization used in [3]. The non-50 Ω signal-source impedance LNA based on the topology in Fig. 1 and implemented in 90 nm bulk CMOS meets the SKA LNA requirements that are shown in Table I and achieves what the authors believe to be the lowest noise figure reported to date for wideband room-temperature CMOS LNAs. To achieve the low noise figures, the work in [5] is generalized to include second-order parasitics by applying a two-port LNA optimization to determine the optimum transistor sizes. The layout issues are discussed and layout details are presented. Measured results of a prototype LNA are presented to verify the theory.

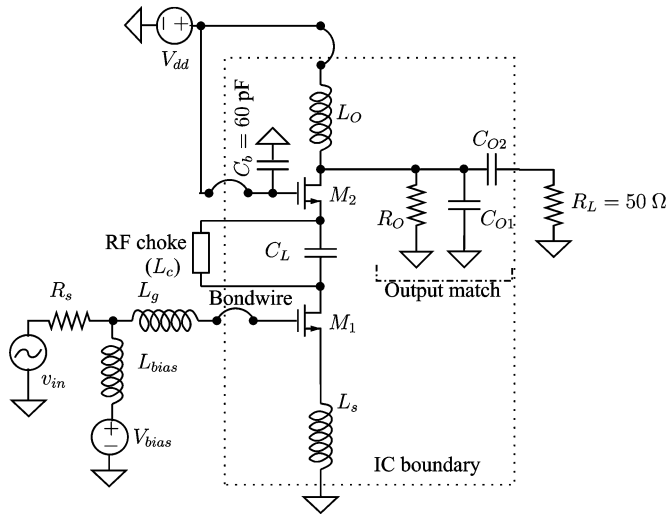

Fig. 1. Wideband LNA circuit diagram.

II. LNA Topology

A wideband LNA based on the topology in Fig. 1 achieves a wide bandwidth by inserting a capacitor C_L between stages of

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TABLE I
SKA LNA SPECIFICATIONS TARGETED AND ACHIEVED IN THIS WORK

Specification	Desired [5], [9]	Achieved in this paper
Frequency	$0.7-1.4$ GHz	$0.7-1.4$ GHz
Noise temperature	20 K max	14 K max[ab] 20 K max[c]
Return loss	10 dB min	11 dB min
Gain, min	15 dB min	17 dB min
IP1dB	-40 dBm min	-18 dBm typ
Power consumption	100 mW typ	43 mW typ

[a]A noise temperature of 14 K corresponds to a noise figure of 0.2 dB at 300 K.
[b]Due to the limit on the source tuner low frequency, measurements with a non-50 Ω signal-source resistance were not performed below 800 MHz.
[c]Measured in the 50 Ω environment from 700 MHz to 800 MHz.

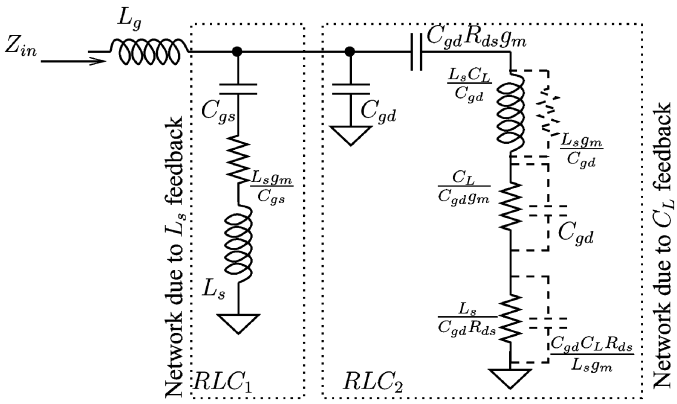


Fig. 2. Resonant structures representing the input impedance of the LNA [9].

a conventional narrowband cascode LNA and exploring feedback of the gate-drain capacitor C_{gd} to realize a wideband input impedance match with low noise figure across the band [9]. The original idea of using the feedback through C_{gd} to broadband LNA input impedance was presented in [10].

The input impedance of a cascode LNA with C_L inserted between the two transistors as in Fig. 1 can be represented by two resonant structures RLC_1 and RLC_2 that result from feedback effects of L_s and C_L, respectively, as shown in Fig. 2[9]. When C_L is tuned to a lower value, the inductance of L_sC_L/C_{gd} decreases, increasing the resonant frequency of RLC_2. A wideband input power match is achieved by tuning C_L such that RLC_2 resonates at the lower band edge while RLC_1 resonates at the upper band edge. In an LNA design, C_L is set to a large value, acting as an AC short, and the LNA is optimized at the upper band edge. Having noise figure optimized at the high-frequency edge allows for the overall best noise figure in the desired band of frequencies since below the frequency of optimization the noise figure is nearly constant but it increases very fast above the frequency at which it was optimized [3], [9]. Once the LNA is optimized, C_L is tuned in the simulator to bring the resonance of RLC_2 in band thus achieving the wideband input power match without affecting the noise figure. Note that in contrast with [3] in which a bandwidth and power constrained optimization was performed, in this paper only the power consumption is constrained and the broadband power match is achieved by using the secondary feedback through C_{gd} [9]–[12].

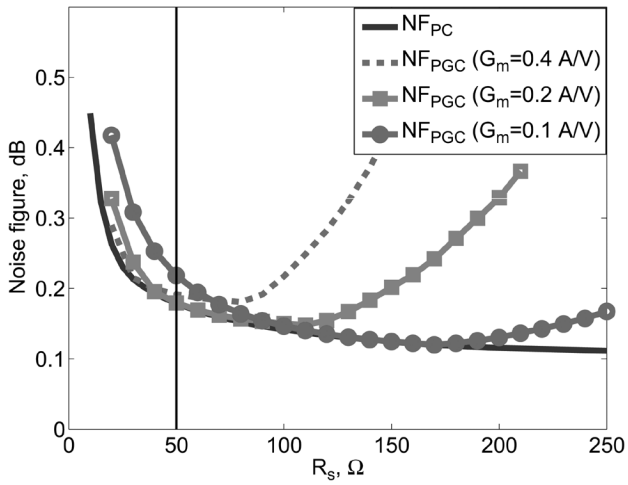


Fig. 3. Representative behavior of the optimized noise figure as a function of signal-source resistance for power constrained optimization (PC) and power and gain constrained optimization (PGC) for three different gains for 90 nm CMOS.

III. EFFECT OF SECONDARY NOISE SOURCES ON NOISE FIGURE OPTIMIZATION

In [5], we modified LNA noise figure optimizations from [13] and showed that adjusting signal-source impedance may lower LNA noise figures. Three different optimizations were identified: power constrained (PC), power/gain constrained (PGC), and power/gain/signal-source resistance constrained (PGRC) optimizations to determine the LNA transistor size and biasing.

In the PC optimization, only LNA power consumption was fixed and the signal-source resistance was swept to determine the optimum value of R_s. Noise figures of LNAs, optimized with the PC optimization that only accounts for the noise due to the transistor and a gate inductor, decrease with the signal source resistance as shown in Fig. 3, and to minimize the noise figure the signal source resistance must be made very large. However, as the power-matched and power-constrained LNA transconductance gain, $G_m = g_m\left(2\omega C_{gs}R_s\right)^{-1}$, decreases due to the increase of R_s, the noise contributions of the cascode transistor and the choke inductor become more and more significant. Due to this, PGC optimization was discussed in [5] that allowed setting of the desired transconductance gain to a fixed value in addition to maintaining fixed power consumption. As the value of R_s was swept, the behavior of the noise figure as shown in Fig. 3 exhibited a noticeable minimum and the optimum R_s could be identified that makes the noise figure lowest given constraints of power consumption and gain. However, the best noise figure achieved with the PGC optimization is not better than that achieved with the PC optimization and therefore, the PC optimization is considered in this paper as it allows greater design flexibility. The discussion in [5] went further using the PGRC optimization by forcing the LNA optimum signal-source resistance for minimum noise to be equal to the signal-source resistance. This, however, resulted in worsening of the noise figure and therefore, PGRC optimization is not considered in this paper.

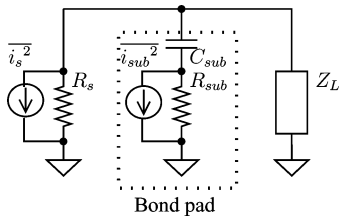


Fig. 4. A simplified model used to estimate the noise contribution of the bond pad. R_s is the signal-source resistance, $C_{\rm sub}$ and $R_{\rm sub}$ are the parasitic element representing the bond pad, and Z_L represents the LNA input impedance. $\overline{i_{\rm sub}^2}$ and $\overline{i_s^2}$ are the thermal noise generators for $R_{\rm sub}$ and R_s.

When the noise model in [5] is expanded by adding the biasing network ($L_{\rm bias}$ at the gate of M_1 in Fig. 1), the noise contribution due to its parallel loss resistance, R_p, will start to dominate at high R_s. When R_p is large, its noise current is much smaller than that of R_s, however, as the two resistances come closer the effect of the biasing network becomes more prominent. When the noise figure of the LNA is of the order of 0.2 dB, in order for the noise contribution of R_p to be insignificant, i.e., contributing less than 10% of the LNA noise power, the following must be achieved:

$$\frac{R_s}{R_p} \leq F_{ex} \tag{1}$$

where $F_{ex} = 10\% \times (10^{0.2\ \rm dB/10} - 1)$, and thus

$$R_p \geq 212 R_s. \tag{2}$$

From (2), as R_s increases, R_p must increase or equivalently the quality factor of $L_{\rm bias}$ must increase to avoid an increase in noise figure.

Similarly, all other parasitic resistances that are insignificant at low R_s may become important noise contributors at high R_s. One of the most prominent of such noise contributors is the bond pad whose noise originates in the substrate and couples capacitively to the RF signal path. In general, it is important to provide very good substrate shielding under all passive components near the input RF path in order to minimize the coupling of the substrate noise [3], [14] and this is even more critical when R_s is high. If the substrate noise of a bond pad is modelled by a noisy resistor $R_{\rm sub}$ and a capacitor $C_{\rm sub}$ as shown in Fig. 4, then the ratio of the mean-square noise voltage, $\overline{v_{L,\rm sub}^2}$, delivered to the LNA input due to $R_{\rm sub}$ and the mean-square noise voltage, $\overline{v_{L,s}^2}$, delivered to the LNA input due to R_s is

$$\frac{\overline{v_{L,\rm sub}^2}}{\overline{v_{L,s}^2}} = \frac{\omega^2 C_{\rm sub}^2 R_{\rm sub} R_s}{1 + \omega^2 C_{\rm sub}^2 R_{\rm sub}^2} \tag{3}$$

where the LNA input is represented by its input impedance Z_L in Fig. 4. From (3), as R_s increases the substrate noise power coupled to the LNA input increases linearly with R_s. To minimize this noise, either $R_{\rm sub} \to \infty$ or $R_{\rm sub} \to 0$[14]. Achieving $R_{\rm sub} \to \infty$ is difficult on a low resistivity substrate whereas $R_{\rm sub} \to 0$ can be achieved by shielding the transmission lines and the bond pads [14]. To set the noise contribution of the substrate under the bond pad below 10% of the total LNA noise when a noise figure of 0.2 dB is assumed, the following needs to be satisfied:

$$\frac{\omega^2 C_{\rm sub}^2 R_{\rm sub} R_s}{1 + \omega^2 C_{\rm sub}^2 R_{\rm sub}^2} \leq F_{ex}. \tag{4}$$

Then $R_{\rm sub}$ can be expressed as a function of R_s when assuming that $C_{\rm sub} = 0.1$ pF for a 100 μm $\times$100 μm bond pad and an operating frequency of 1.4 GHz as

$$R_{\rm sub} \leq \frac{R_s}{2F_{ex}} \left(1 - \sqrt{1 - \frac{4F_{ex}^2}{\omega^2 C_{\rm sub}^2 R_s^2}}\right) \tag{5}$$

$$\lesssim \frac{F_{ex}}{\omega^2 C_{\rm sub}^2 R_s} = \frac{6 \times 10^3}{R_s}. \tag{6}$$

Reduction of $R_{\rm sub}$ can be achieved by shielding as will be shown in Section VI. Similar analysis applies to the trace connecting the gate of the main transistor M_1 to the bond pad and other passive circuit components.

IV. Transistor Modelling

In this paper, the transistors were modelled with the second-order model from [15]. The model is often used as it allows designers to analytically relate power consumption to transistor small-signal parameters [13], [16]. To improve the modelling accuracy and the match between the second-order model and the BSIM model, the second-order model was adjusted by a small offset in the threshold voltage, $\Delta V_T = 15$ mV, and a small offset of $\Delta g_m = -116\,\mu$A/V, in the values of I_d and g_m where

$$I_d = W C_{ox} v_{\rm sat} \frac{V_{od}^2}{V_{od} + L E_{\rm sat}} \tag{7}$$

and

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \mu_{\rm eff} C_{ox} \frac{W}{L} V_{od} \frac{1 + \frac{1}{2}\rho}{(1+\rho)^2} + \Delta g_m N \tag{8}$$

N is the number of gate fingers, $\rho = V_{od}/L E_{\rm sat}$, the overdrive voltage $V_{od} = V_{gs} - (V_T - \Delta V_T)$, V_T is the threshold voltage, V_{gs} is the gate-source voltage, W and L are the transistor gate width and length, $E_{\rm sat}$ is the velocity saturation field strength, $v_{\rm sat}$ is the saturation velocity, C_{ox} is the gate oxide capacitance per unit area, and $\mu_{\rm eff} = 2v_{\rm sat}/E_{\rm sat}$. The other parameters were related to the power consumption through the transistor width. Note that the small offsets ΔV_T and Δg_m in the second-order model were found for a typical transistor that was expected to be used in the LNA presented later in this paper. The authors do not claim that these offsets are valid for any transistor size nor do the authors claim any physical meaning to these offsets.

Recent work [17] has indicated that perhaps the noise parameters of the 90 nm CMOS process are only marginally larger than the noise parameters of a long-channel transistor. Therefore, in contrast with work in [3], the long-channel transistor noise parameters for drain-noise current $\gamma = 2/3$ and gate-noise current $\delta = 4/3$ with the correlation coefficient $c = j0.395$ were used to model the transistor noise currents in this paper. Based on our measurements, the approach of using the long channel noise parameters yields good results.

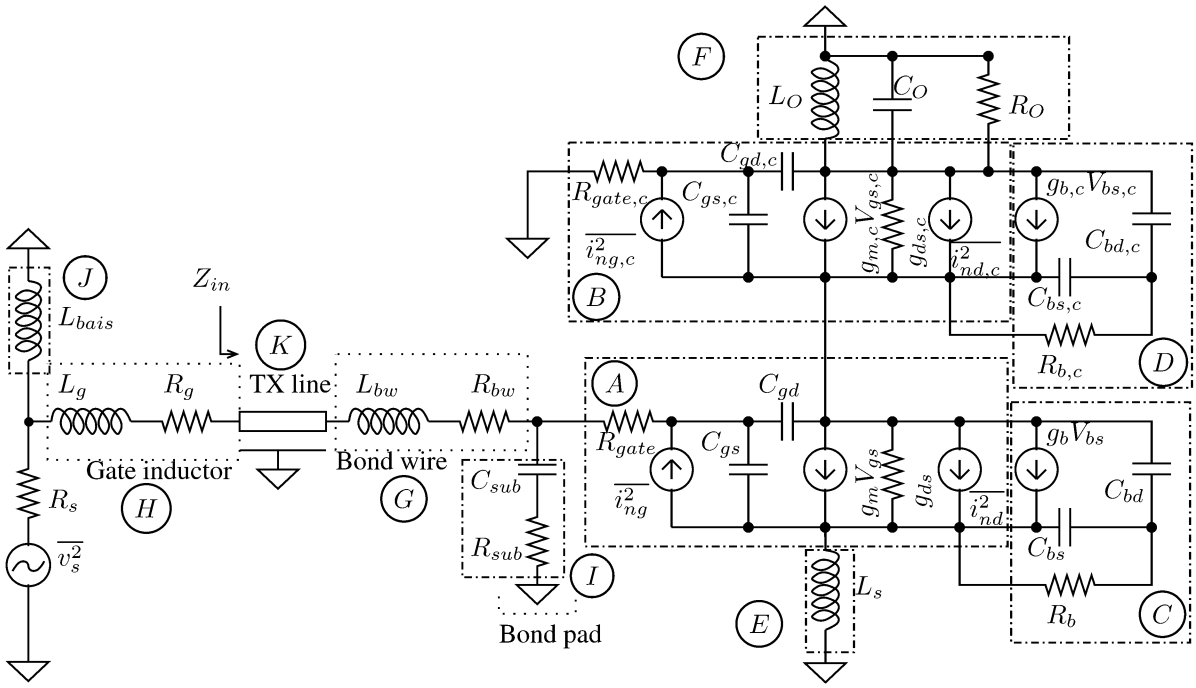


Fig. 5. Two-port LNA model. PCB trace indicated in the figure with "TX line" is located on the printed circuit board between the soldered gate inductor and the bond wire. The two-port sub-modules are labelled with $\odot$.

V. Optimization Procedure

The optimization follows the noise optimization approach in [5] but to improve the model accuracy the transistors are modelled with their two-port representations to calculate the input impedance and noise figure more accurately. The two-port model shown in Fig. 5 incorporates (7) and (8), and second-order components such as C_{gd} and the transistor bulk networks that were not included in the optimization in [5].

Following the PC optimization curve in Fig. 3 would suggest that the higher the R_s the lower the noise figure. However, addition of other second order parasitics, the noise due to the cascode transistor, and the RF choke to the PC optimizations results in the appearance of an optimum $R_s = R_{s,\mathrm{opt}}$ that minimizes the LNA noise figure. In contrast with the ideal PC optimization in Fig. 3, the LNA noise figure increases at $R_s > R_{s,\mathrm{opt}}$. This will be now demonstrated.

Once the second order model is created numerically by using the two-port theory [18]–[20], the value of the source degeneration inductor L_s is swept and the input impedance Z_{in} indicated in Fig. 5 is calculated for an array of overdrive voltages V_{od} at the high-frequency band edge. For input power match, ignoring large L_{bias}, the following condition must be satisfied:

$$\begin{cases} \Im\{Z_{\mathrm{in}}(\omega_0)\} + R_g Q_{\mathrm{ind}} = 0 \\ \Re\{Z_{\mathrm{in}}(\omega_0)\} + R_g = R_s \end{cases} \tag{9}$$

and therefore

$$\begin{cases} \Re\{Z_{\mathrm{in}}(\omega_0)\} - \Im\{Z_{\mathrm{in}}(\omega_0)\}\frac{1}{Q_{\mathrm{ind}}} = R_s \\ R_g = R_s - \Re\{Z_{\mathrm{in}}(\omega_0)\} \end{cases} \tag{10}$$

can be used to find $R_g(V_{od}, L_s)$ from which, with the knowledge of the quality factor of the gate inductor Q_{ind}, $L_g(V_{od}, L_s)$ is found and the noise factor $F(V_{od}, L_s)$ is determined. At the end of the L_s sweep the overdrive voltage and L_s that result in the lowest noise factor are selected. This procedure is repeated for several values of R_s and the value of R_s that gives the lowest noise factor is selected for the LNA design. Fig. 6 shows simulated noise figures of optimized LNAs for different values of R_s ranging from 50 Ω to 200 Ω. In this optimization, a high-quality CoilCraft gate inductor, L_g, was selected with $Q \approx 100$, and $L_{\mathrm{bias}} = 47$ nH and $L_c = 100$ nH were also implemented as external inductors with their quality factors > 60. L_c was located off-chip mainly to confirm the independence of the noise figure on C_L. L_{bias} was selected such that its parasitic parallel resistance agreed with that found with (2). When the LNA is integrated with the telescope L_{bias} will be either replaced with an on-chip resistor or integrated into the transmission line connecting the antenna and the LNA. Inductor L_g must be placed off-chip if the LNA is to meet the SKA requirements as the on-chip inductor quality factors are too low. In the future, L_g may become a part of the antenna–LNA interconnect.

Once the narrowband LNA is optimized at the high-frequency band edge, the value of C_L is tuned in the simulator to shift the resonance point of the input impedance such that adequate return loss is achieved across the band of interest without a significant impact on the noise figure [9] as is verified later in this paper in Fig. 12. In contrast with conventional wireless devices, for radio astronomers the relatively small improvement in the noise figure shown in Fig. 6 at nonstandard signal-source resistance is significant and it represents a 2 K improvement in the noise temperature, 10% of the specified maximum noise temperature for this LNA.

The simulations do not suggest that increasing R_s only adds measuring difficulties with no significant noise figure advantage

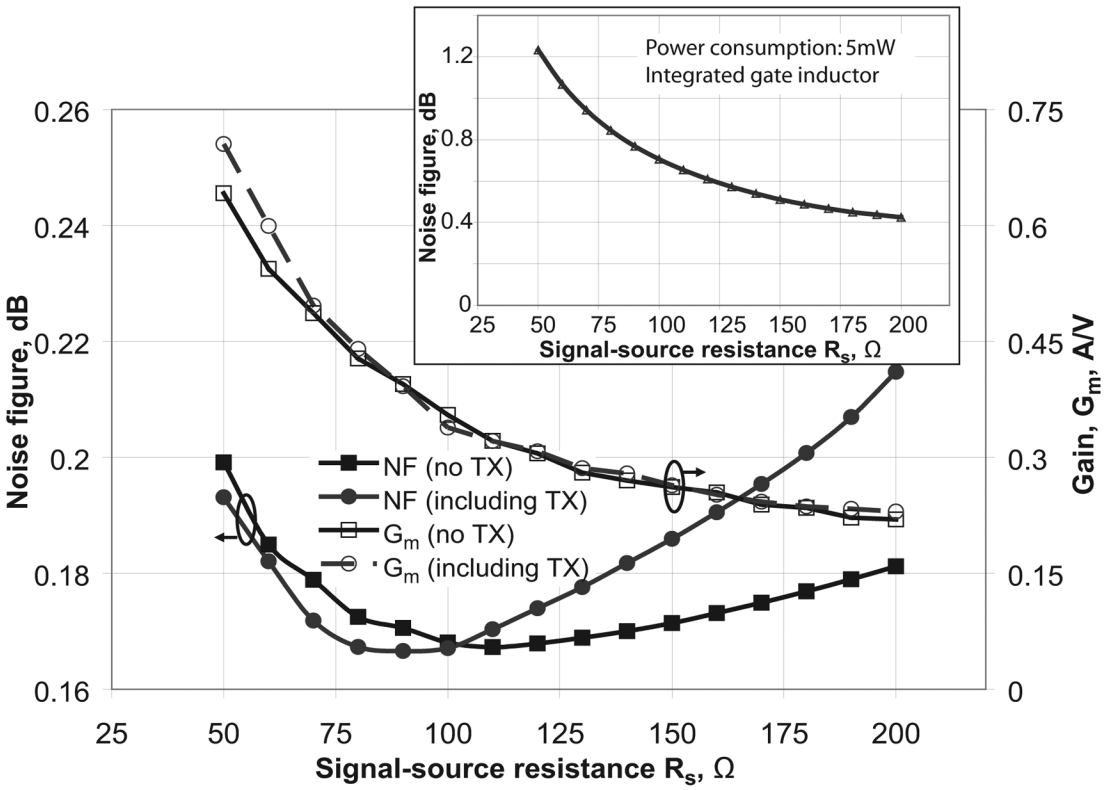


Fig. 6. Simulated noise figures of LNAs optimized for a number of signal-source resistances between 50 Ω and 200 Ω with the power consumption fixed at 50 mW. In contrast with Fig. 3 the power constrained optimization shows an optimum value. The LNA gain is defined as $G_m = g_m(2\omega C_{gs}R_s)^{-1}$. Dependence of the noise figure and G_m on R_s are shown for two cases. In one case a PCB trace, "TX line" in Fig. 5, was omitted giving $R_{s,\mathrm{opt}} = 110\ \Omega$ and in the other case it was included resulting in $R_{s,\mathrm{opt}} = 85\ \Omega$ [see Section VII]. The insert shows simulated noise figures achieved with LNAs optimized for different R_s when the power consumption is fixed at 5 mW and the gate inductor is integrated ($Q = 5$).

for commercial applications. The insert in Fig. 6 shows noise figures of LNAs optimized at various values of R_s but in this case the gate inductor is integrated and has $Q = 5$ and the power consumption of the LNAs is constrained to 5 mW. There is a 0.5 dB improvement in the noise figure, corresponding to 45% of noise temperature change, when $R_s = 100\,\Omega$ is selected rather than the standard $R_s = 50\ \Omega$.

VI. Layout Issues

The importance of substrate shielding has been highlighted experimentally in [3] where a noise figure increase of > 0.1 dB was measured in an LNA that did not employ substrate shielding. In this design all passive components were shielded to avoid substrate noise pick up. The bond pads and the capacitors were shielded with a solid n^+-implant as in [14] to reduce R_{sub} as required by (6). Inductors were shielded with patterned ground shields [21]. An example of the shielding employed under the lines carrying the RF signals is shown in Fig. 7. The transmission line shown in the middle of the drawing in Fig. 7 was surrounded by grounded metal paths. All metal layers, connected with a large number of vias, were used for the ground paths. On the lowest metal layer thin metal strips were added to connect the two ground paths, provide shielding of the substrate, and to reduce the losses in the transmission line. In [22], it has been shown that these strips effectively shield the lossy substrate in the frequency range of interest, resulting in less noise added to the RF signals internal to the

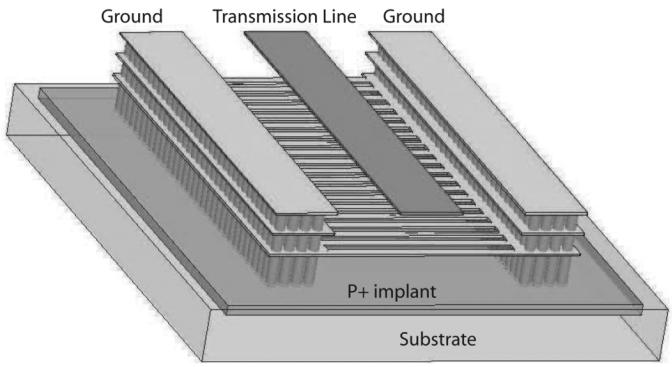


Fig. 7. Representation of the substrate shielding. The drawing is not to scale.

LNA. The complete ground network was abundantly connected to the substrate. Any ground current that would flow through the substrate would be soaked up by the low resistance path through the ground structure, thus limiting the resistance in the ground current path. A large number of ground bond pads were connected together and bonded to the circuit board. This provides a low impedance path for RF ground currents between the grounds on the die and the circuit board. All grounded structures were well interconnected to minimize the resistance path for the RF ground currents and the substrate was abundantly contacted.

The wide transistors required by the LNA were broken into eight unit transistors with many gate fingers used and placed in a

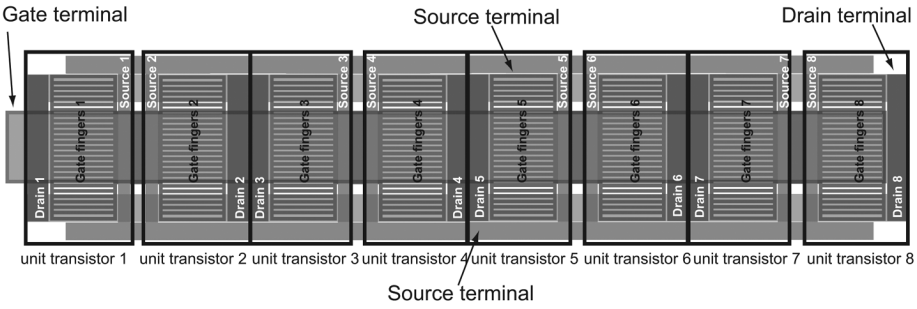


Fig. 8. Transistor layout. Shown gate, drain, and source interconnects utilize seven metal layers. The gate interconnect also employed the aluminum cap layer to further reduce parasitic gate resistance. All metal traces are connected with the maximum number of vias allowed by the design rules. Only representative connections are shown due to complicated multilayer interconnections used in the layout.

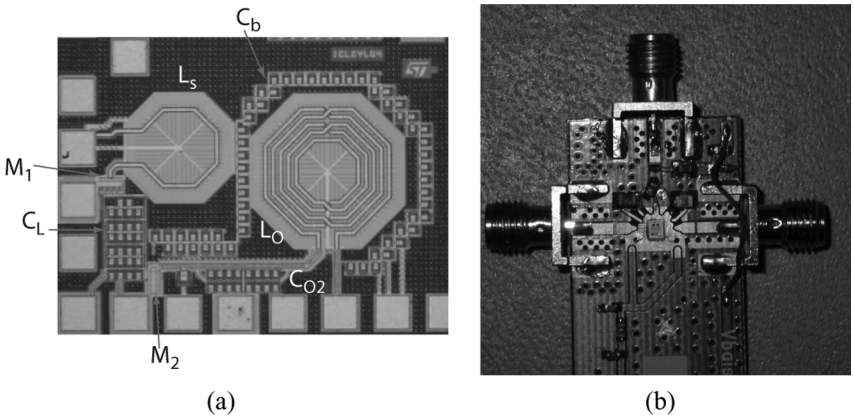


Fig. 9. (a) Die photograph. The LNA dimensions are 1100 μm$\times$750 μm including the bond pads. (b) LNA die bonded to a circuit board.

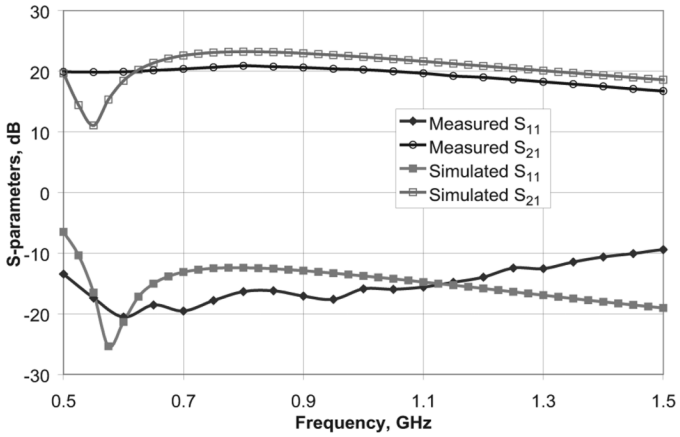
matrix configuration as shown in Fig. 8. In addition to reducing the noise from parasitic resistances, the matrix configuration allows the splitting of the DC current such that the maximum current density for each of the metals used in the transistor layout is not violated. Similar approaches to subdividing the transistor into unit cells were successfully employed in [3], [23].

A large bypass capacitor C_b shown in Fig. 1 was implemented using a number of shunt MIM-capacitors in parallel. The capacitor C_b, identified in Fig. 9 and used to improve stability, is laid out around the choke inductor L_O and in this way it does not add to the LNA die area significantly.

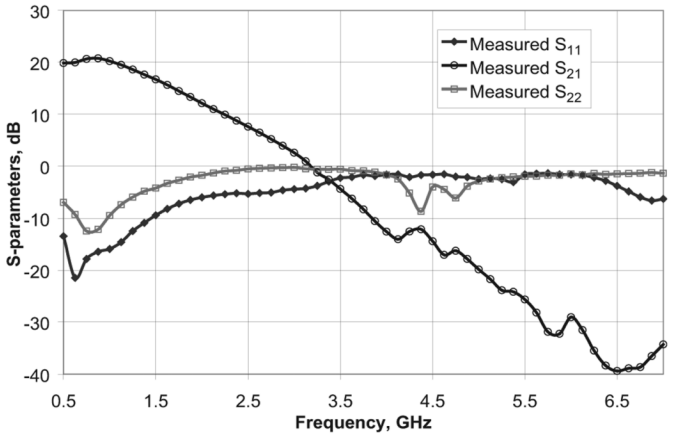
VII. Measurement Results

The fabricated die, shown in Fig. 9, was wirebonded onto a circuit board [see Fig. 9(b)] and measured in a shielded enclosure in a shielded room. During the design stage, the effect of a short PCB trace between the gate inductor and the gate bond wire on the input impedance was underestimated. This trace modifies input impedance and results in optimum $R_{s,\mathrm{opt}} = 85\ \Omega$ rather than $R_{s,\mathrm{opt}} = 110\ \Omega$ for both the noise match and power match [see Fig. 6] and makes the fabricated LNA slightly suboptimum. To find $R_{s,\mathrm{opt}} = 85\ \Omega$, the LNA optimization from Section V was repeated and fortuitously resulted in virtually identical design to the original design that resulted in $R_{s,\mathrm{opt}} = 110\ \Omega$. Measured S-parameters are presented in Fig. 10(a) overlaid on top of the simulated values that do include the PCB trace. In Fig. 10(b), the parameters measured over a wide frequency range are shown. In both plots in Fig. 10, $R_s = 85\ \Omega$ and $R_L = 50\ \Omega$.

The noise measurement system, described in the Appendix, performs the "cold" noise test [24], [25] using Focus Microwave's 1806-CT mechanical source tuner. The lowest operating frequency of the source tuner is limited to 800 MHz. To assess the noise figure below 800 MHz, a 50 Ω N4000A noise source with an N8975A noise figure meter that uses a less accurate "hot–cold" noise measurement was employed [26]. Noise figure measurement results are presented in Fig. 11. The measured results of the noise figure in the 50 Ω environment are shown in Fig. 12. Impact of C_L on the noise figure was assessed by shorting inductor L_c, which acts as an RF choke [see Fig. 1]. As shown in Fig. 12, the LNA gain and noise figures are affected below 800 MHz. However, over the rest of the band there is no significant difference in the two parameters as expected [3], [9]. The optimum source admittance, Y_{opt}, for minimum noise and the equivalent noise resistance, R_n, were also measured for frequencies between 0.8 GHz and 1.4 GHz and are shown in Figs. 13 and 14. Variations of Y_{opt} are attributed to the uncertainties in curve fitting. These uncertainties become larger as the value of R_n decreases since small R_n shown in Fig. 14 reduces LNA sensitivity to signal-source impedance [27]. The reason for curve fitting in the "cold" noise measurement method and the impact of the measurement scatter on the accuracy of the noise figure measurements are discussed in the Appendix.



(a)



(b)

Fig. 10. (a) Measured and simulated S-parameters when $R_s = 85\ \Omega$ and $R_L = 50\ \Omega$. (b) Measured S-parameters over a wide frequency range when $R_s = 85\ \Omega$ and $R_L = 50\ \Omega$. PCB trace was included in the simulations.

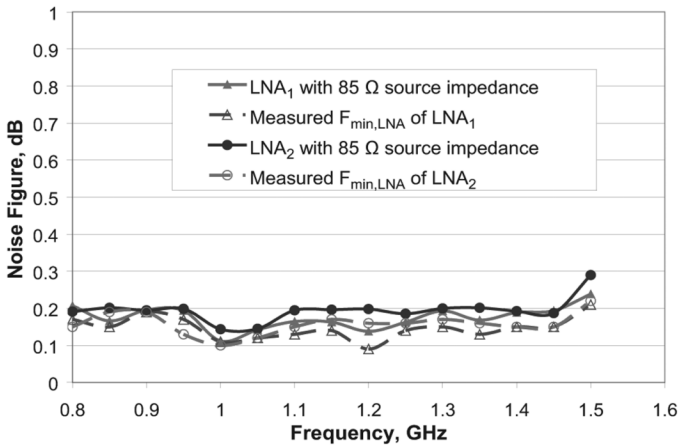


Fig. 11. Measured $F_{\min,\mathrm{LNA}}$, noise figure with $R_s = 85\ \Omega$ for two different LNAs. $F_{\min,\mathrm{LNA}}$ represents the minimum noise figure the LNA can achieve.

The linearity of the LNA was measured with 50 Ω equipment at 1 GHz and is reported in Fig. 15. The LNA achieves output P1dB of 2 dBm, output IP3 of 12 dBm, and output IP2 of 22 dBm. The power consumption of the LNA is 43 mW from a 1 V supply.

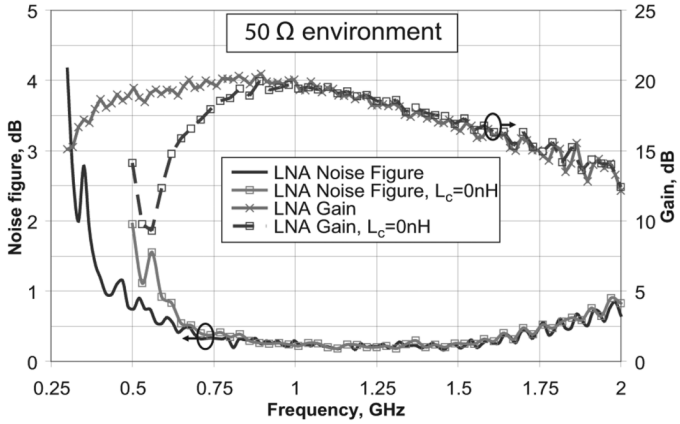


Fig. 12. Noise figure measurement with a 50 Ω N4000A noise source and an N8975A noise figure meter. One of the measured LNAs had its external RF choke, L_c, short circuited to verify the independence of the noise figure on C_L.

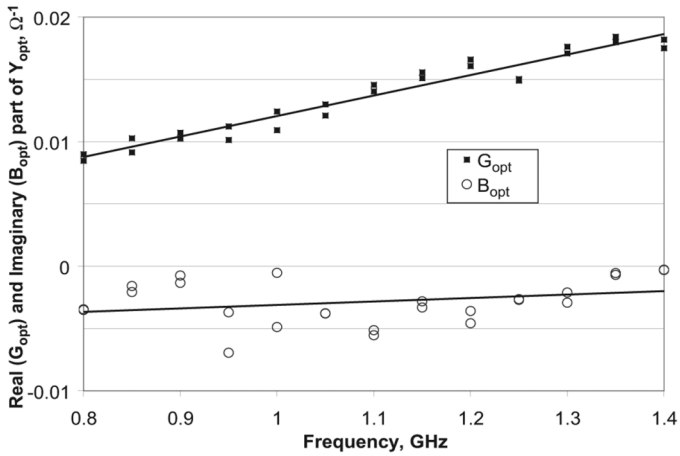


Fig. 13. Measured optimum source admittance, Y_{opt}, for minimum noise for the two LNAs.

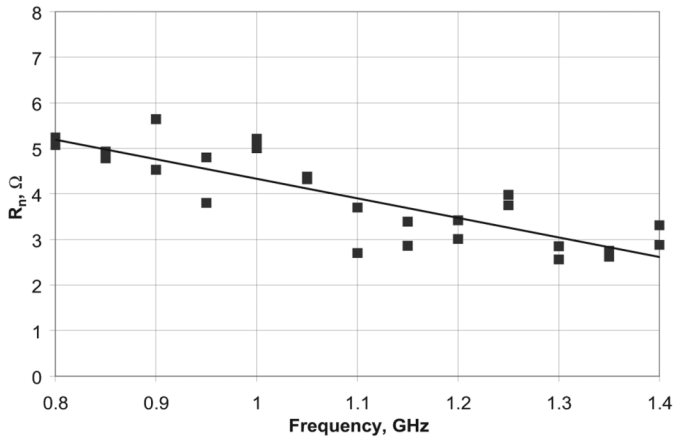


Fig. 14. Measured equivalent noise resistance, R_n, for the two LNAs.

VIII. Conclusion

This paper presented a wideband room temperature LNA designed in 90 nm bulk CMOS that achieves sub-0.2 dB noise figure from 800 to 1400 MHz. The paper discussed the layout issues and the optimization issues related to the design of the LNA. The targeted application of this design is for the SKA

TABLE II
MEASURED PERFORMANCE OF LNAS DESIGNED IN THIS WORK AND COMPARISON OF THE ACHIEVED PERFORMANCE WITH OTHER PUBLISHED DESIGNS TARGETED FOR THE SAME APPLICATION

Specification	This work ($R_s = 85\,\Omega$)	[3] ($R_s = 50\,\Omega$)	[28] ($R_s = 50\,\Omega$)	[8] ($R_s = 150\,\Omega$)	[8] ($R_s = 50\,\Omega$)	[29] ($R_s = 50\,\Omega$)
Technology	CMOS 90 nm	CMOS 90 nm	GaAs 0.15 μm	CMOS 0.18 μm	CMOS 0.18 μm	GaAs 0.2 μm
Frequency[a]	0.7–1.4 GHz	0.7–1.4 GHz	0.7–1.4 GHz	0.3–1.4 GHz	0.8–1.8 GHz	0.6–1.6 GHz
Noise temp.	14 K max[bc] 20 K max[e]	25 K max[d]	22 K max	44 K max	77 K max	35 K max
Input S_{11}	-11 dB max	-15 dB max	not specified	not specified	not specified	-12 dB max
Power gain	17 dB min	16 dB min	18 dB min	26 dB min	23 dB min	21 dB min
IP1dB	-18 dBm typ	-23 dBm typ	not specified	-22 dBm typ[f]	-18 dBm typ[f]	-15 dBm typ[f]
DC power	43 mW typ	45 mW typ	30 mW typ	90 mW	90 mW	852 mW typ
Meas./Sim.	Measured	Measured	Measured	Simulated	Measured	Simulated

[a]Frequencies differ slightly for different telescope prototypes.
[b]A noise temperature of 14 K corresponds to a noise figure of 0.2 dB at 300 K.
[c]Due to the limit on the source tuner low frequency, measurements with a non-50 Ω signal-source resistance were not performed below 800 MHz.
[d]A noise temperature of 25 K corresponds to a noise figure of 0.35 dB at 300 K.
[e]Measured in the 50 Ω environment from 700 MHz to 800 MHz.
[f]Estimated based on IP3.

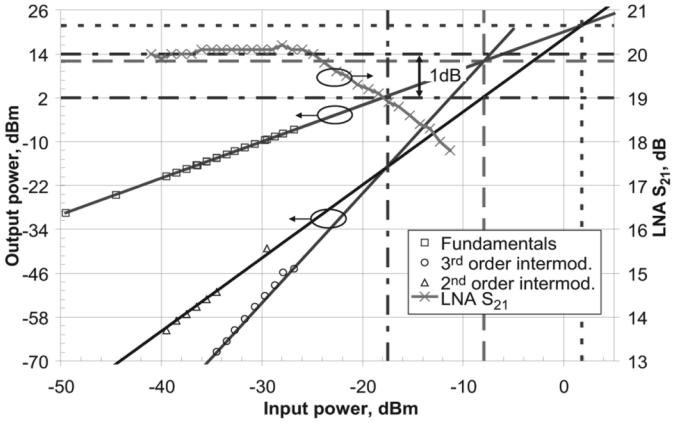


Fig. 15. Linearity measurement of the LNA. Measurements were performed at 1 GHz with 50 Ω equipment. The two fundamental frequencies in the IP3 and IP2 tests were spaced by 2 MHz.

radio telescope. The LNA was designed for a non-50 Ω antenna impedance and passes all specifications for the SKA LNA as shown in Table I. In contrast with the work in [3], this LNA was designed based on long channel noise parameters and using a power constrained noise figure optimization, both of which resulted in a reduction of the noise figure. This LNA outperforms the current state-of-the-art CMOS LNA in [3] and also outperforms equivalent designs as summarized in Table II.

This work shows that an SKA LNA optimization must be conducted in conjunction with the design of the circuit board on which the LNA is to be mounted in order to achieve the best noise figure.

The integration of the LNA and the SKA antenna elements is the subject of future research that will address non-purely-resistive antenna impedance and its effect on the LNA performance and LNA optimization. At that time, the external inductors L_g and $L_{\rm bias}$ may be replaced with the planar structures connecting the antenna and the LNA, and the inductor L_c will be integrated on-chip.

APPENDIX

The "hot–cold" noise figure measurement method used in commercial noise figure meters, although well understood is not very accurate [30]. Since the noise figure of an amplifier depends on the signal-source impedance, the "hot–cold" method used by noise figure meters will be inherently inaccurate as it does not measure the device under test (DUT) and the noise source impedances. In addition, the noise source's impedance changes as it toggles from the ON state (hot) to the OFF state (cold) further adding to errors in the measurements. Combination of all errors in a noise figure measurement with the noise figure meter results in measurement errors in the order of 0.15 dB [30], not satisfactory for the application discussed in this paper. In addition, this method does not allow the determination of the noise parameters (R_n, $Y_{\rm opt}$, and $F_{\rm min}$) of the LNA and only allows the noise figure measurement at $R_s = 50\ \Omega$.

In order to measure the noise parameters using the "hot–cold" method, an impedance tuner, sometimes implemented as a coupler with a few termination standards [31], can be inserted between the noise source and the DUT. The tuner acts as a matching network transferring the noise source output impedance to a sufficient number of complex impedances [25]. These impedances along with the S-parameters of the DUT must be measured with a network analyzer prior to the noise figure measurement. At each of the impedances, the noise figure is measured with the noise figure meter. Once the set of noise figures at the input impedances is obtained, the noise parameters of the DUT are obtained by fitting the general expression of the noise factor

$$F = F_{\rm min} + \frac{R_n}{G_s}\left|Y_s - Y_{\rm opt}\right|^2 \tag{11}$$

to the data set. Although this technique is an improvement of the standard "hot–cold" method, this method relies on the very accurate knowledge of the insertion loss of the network between

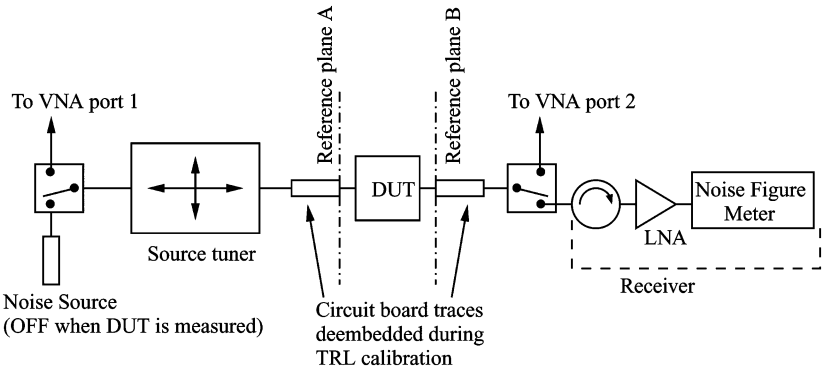


Fig. 16. Block diagram of the noise measurement system.

the noise source and the DUT. This network includes the tuner, cables, and connectors.

Due to the limitations of the "hot–cold" method, in this paper a more accurate "cold" method was used [24], [25]. The main advantages of the "cold" method, described in the rest of the Appendix, are that it accounts for the S-parameters and return losses of all components comprising the measurement system, allows the measurement of the DUT's noise parameters as well as the measurement of the noise figures for varying signal-source impedance, and its errors are mainly related to the accuracy of the network analyzer calibration rather than less accurate noise figure meter calibration.

In this system, a Focus Microwave 1806-CT mechanical source tuner was used. The measurement starts with a very careful calibration of the vector network analyzer (VNA), Agilent's PNA E8363B, with a precision TRL (Thru-Reflect-Line) kit. The network analyzer calibration is very important for this noise measurement method as the measured noise figure is related to the calibration accuracy [32]. Once the VNA is calibrated, calibration of the rest of the noise measurement system is as follows:

1) The impedance of the noise source is measured for both the ON state and the OFF state with the VNA.
2) To account for imperfections of the switches, two TRL calibrations that shift the measurement plane to the input and output of the DUT (reference planes A and B in Fig. 16) are performed. In the case of the LNA described in this paper the DUT input is the input to inductor L_g. The first of the two TRL calibrations determines the S-parameters of the network between the noise source and reference plane A as well as the S-parameters of the network between the output of the DUT (reference plane B in Fig. 16) and the receiver input. The second calibration determines the S-parameters of the network between the VNA port 1 (see Fig. 16) and reference plane A as well as the S-parameters of the network between the reference plane B and the VNA port 2. The first set of S-parameters is used to de-embed the network between the DUT and the receiver during the noise figure measurements and to measure the receiver input impedance. The last set of the S-parameters is used to de-embed the networks between VNA ports and the DUT during *in situ* DUT S-parameter measurements and is also used to de-embed the network between the reference plane A and the VNA port 2 during tuner calibration when the tuner's output impedance is measured.
3) During the tuner calibration, with the DUT replaced by the "Thru" calibration standard, the noise source is turned OFF and the tuner is manipulated to present a large number of impedances at reference plane A as shown in Fig. 17. These impedances are measured with the network analyzer and are important for the "cold" noise measurement method as they permit the extraction of the noise parameters of the DUT and the receiver.
4) The last important step in the calibration procedure is the calibration of the receiver noted in Fig. 16. This calibration is performed by using the "hot–cold" method described above to measure the receiver gain. The noise source is then turned OFF and the "cold" noise measurement method is used to determine the receiver's noise parameters. To obtain the receiver noise parameters, the tuner is controlled to present a set of impedances to the receiver input. The noise figure of the receiver is obtained at each tuner impedance by measuring the receiver's output power and referencing it to the input power generated by the real part of the tuner's output impedance. The noise figures and the associated tuner impedances are used to obtain the receiver noise parameters by fitting (11) to the data set [33].

Once the receiver's noise parameters are measured, the DUT is inserted and its noise parameter measurement proceeds by using the tuner to present a number of different signal-source impedances, sufficient to fit (11) to measured data, and measuring the corresponding output powers with the calibrated receiver. With the accurate knowledge of the input noise powers which were measured during the tuner calibration with the VNA while the noise source is turned OFF, the noise figure is calculated and the noise parameters are extracted by fitting (11) to the measured data [33]. An example of this measurement is shown in Fig. 17 where the signal-source impedances presented by the tuner to the LNA during noise parameter extraction are noted with "+" and the extracted $F_{\min}$ and its location and the noise circles based on the extracted R_n are presented.

The noise figure measurement system was verified by measuring the noise figure of a 0.1 dB attenuator and the "Thru" calibration standard. Fig. 18 shows the measured noise figures and the insertion loss measured with the VNA. In this figure, the errors in the noise figure measurements do not exceed 0.09 dB.

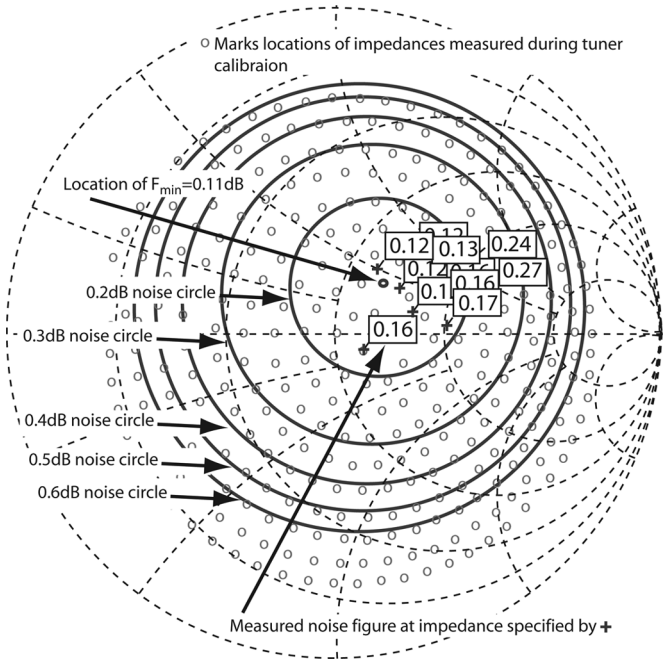


Fig. 17. Typical outcome of a noise measurement process. Impedances measured during the tuner calibration are shown with "o" and the noise figures measured for eleven impedances, marked with "+", are shown. Due to the locations of the impedances only some locations are visible in this figure. The location of the minimum noise figure on the Smith chart is shown and corresponds to $Y_{\rm opt}$. The noise circles are also shown and identified. During LNA measurements the tuner was calibrated at 1200 different impedances whereas in this figure the tuner was calibrated at 300 different positions to improve figure readability.

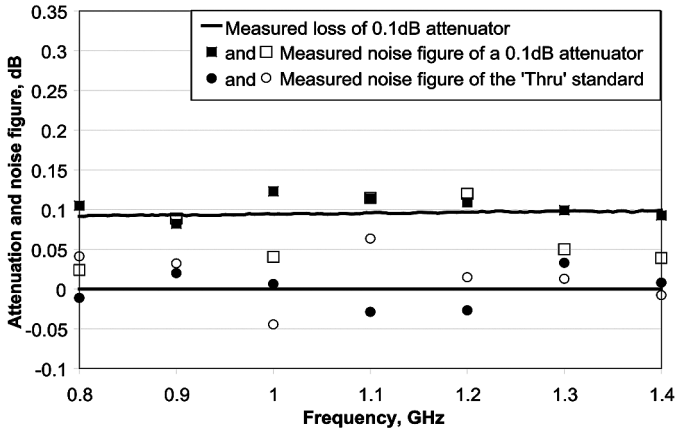


Fig. 18. Noise figure verification results for two sets of measurements with the system recalibration in between. For the measurements labelled with "□" and "o" the noise source was only used during the receiver calibration and it was replaced with a passive 50 Ω termination during the noise figure measurement.

This result is consistent with the tuner manufacturer documentation and is dominated by the receiver calibration accuracy [34]. When a DUT with gain is measured, the accuracy of the receiver calibration becomes less significant. To assess the uncertainties in more detail, the receiver was then recalibrated with a smaller number of input impedances presented by the tuner, therefore modifying the accuracy of the receiver calibration due to fewer data points available for fit of (11) and determination of the receiver noise parameters. Two noise sources were used. These measurements were repeated a number of times at a single frequency. The average error in the noise figure relative to the loss was found to be 0.035 dB with a standard deviation of 0.042 dB. Although these errors appear large, during noise figure measurements of a DUT with a large gain, >18 dB in the case of the LNA discussed in this paper, the errors in the receiver calibrations will be largely suppressed. The dominant source of uncertainty remaining is related to the accuracy of the network analyzer calibration and the S-parameter measurement of the network between VNA port 2 and the reference plane B. To control these remaining uncertainties, these measurements are continuously reassessed by analyzing the measured S-parameters and verifying that a difference between $|S_{21}|$ and $|S_{12}|$ is not greater than 0.001 dB for all passive structures. In addition it must be verified that the phases of the S-parameters do not have discontinuities and follow smooth trajectories.

To analyze the measurement scatter, we assume that the scatter is independent of frequency [31] and uncorrelated, once the first-order linear frequency dependence is removed. Note that the simulated $F_{\rm min}$, $Y_{\rm opt} = G_{\rm opt} + jB_{\rm opt}$, and R_n exhibit nearly linear frequency dependence. To remove the first-order linear dependence, we fit straight lines to the measured $F_{\rm min}$, $Y_{\rm opt}$, and R_n of two LNAs, shown in Figs. 11, 13, and 14, and subtract the fitted lines from $F_{\rm min}$, $Y_{\rm opt}$, and R_n to obtain the measurement scatter. Standard deviations, $\sigma_{\rm Fmin}$, $\sigma_{\rm Yopt}$, and σ_{Rn} for the scatter in the measurements of $F_{\rm min}$, $Y_{\rm opt}$, and R_n respectively, are then calculated. The expected standard deviation in the noise factor measurements, σ_F, is found by solving

$$\sigma_F^2 = \sigma_{\rm Fmin}^2 \left(\frac{\partial F}{\partial F_{\rm min}}\right)^2 + \sigma_{Rn}^2 \left(\frac{\partial F}{\partial R_n}\right)^2 + \sigma_{\rm Yopt}^2 \left(\frac{\partial F}{\partial Y_{\rm opt}}\right)^2 \tag{12}$$

where F is expressed in (11). With (12), we find that the maximum expected standard deviation in the LNA noise figure measurements due to measurement equipment uncertainties and due to LNA performance variability when converted to decibels for a 0.2 dB noise figure does not exceed 0.035 dB. In addition, based on our experience with assembling and calibrating the test system, we find that the measurement repeatability is within ±0.03 dB.

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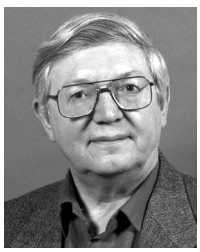

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