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Product Note No 18

Design Verification Software - DVP

DVP is a CCMT Application that permits to Verify, by Measurement, the performance of an MIC or MMIC amplifier using the same chip or packaged transistor the design has been based on.
DVP reads data in S2P (ASCII) format from linear or nonlinear network analysis programs and synthesizes source and load impedances, over a wide frequency range, using the programmable tuners. This permits to **measure** the **future** circuit and **check its performance before the first iteration.**

Introduction

An on going concern of any design cycle is how close the final circuit will be to the predicted performance. This depends mostly on the design method and the data used. This data are S-parameters of active devices (transistors) and passive components (microstrip in general). The S-parameters can be obtained from direct (small signal) measurements on a Network Analyzer or numerical models of passive circuits. For high power designs data for the active devices can be obtained from Load Pull measurements or from nonlinear device models.

While small signal designs have reached maturity, due to accurate models and S-parameter measurement techniques, the large signal designs are still a matter of concern.
Either the measured data are not available at exactly the required conditions or the nonlinear models are not accurate enough for hard saturation.
In any case the design of a power amplifier still tends to be a matter of several "iterations" which can also be considered as "design failures".
A **"first pass" design** is the aim of development activities in a number of laboratories.

The Design Verification technique, described here, does not improve the design as such. It rather aims to avoid costly "iterations" of designs which are destined to fail, for whatever reason, either due to wrong data or even a mistake or negligence of some, at first sight, secondary detail, like bias networks, packaging, assembly or even thermal effects, some of which can easily be modeled and some not.

This note describes the DVP method step by step and presents evidence of its usefulness.

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Description of DVP

An amplifier is an active device (transistor) loaded on the input and output ports by some, frequency dependent impedances. These impedances are generated by some matching networks, which also have some loss. The gain of the transistor under the actual matching conditions minus the actual loss of the matching networks gives the gain of the total amplifier.

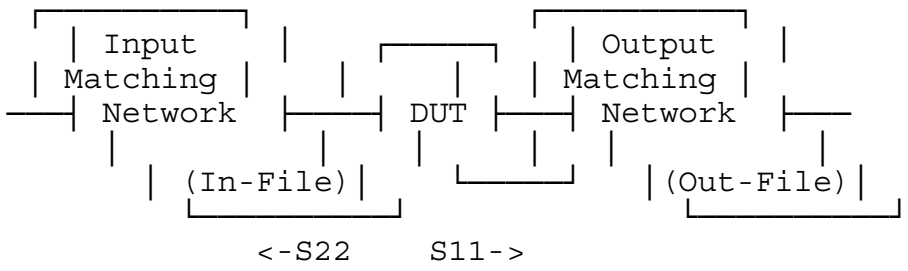


Figure 1: Schematics of a single stage Amplifier

The gain of the transistor (DUT) at a given frequency depends on the following parameters:

1- Bias conditions
2- Input power
3- Source and Load impedance.

It does not depend, however, on the loss of the matching networks. The loss of the matching networks interferes only with the overall amplifier gain.
If we can test the transistor under the same source/load impedance conditions, the same input power and bias conditions we should be able to measure its actual gain in a circuit
that has not been manufactured yet.
In order to be able to compare the gain of the load pull setup with the gain of the amplifier we therefore have to refer the load pull measurement back to the gain of the transistor in the amplifier environment.

This can be done using two programmable (preferably low loss) tuners, that can accurately fine tune to any impedance within the Smith Chart (figure 2).
The setup shown on figure 2 uses two CCMT tuners and is capable of synthesizing any impedance on the Smith Chart (within the calibration range of up to 20:1 VSWR).
The impedances to be tuned to can either be clicked in using the mouse, entered via keyboard, or, as in the case of Design Verification, be transferred to the CCMT software using an ASCII (S2P) file from another computer or simulator programm.

Figure 2 shows the principle of a load pull setup capable of operating the DVP test routine.

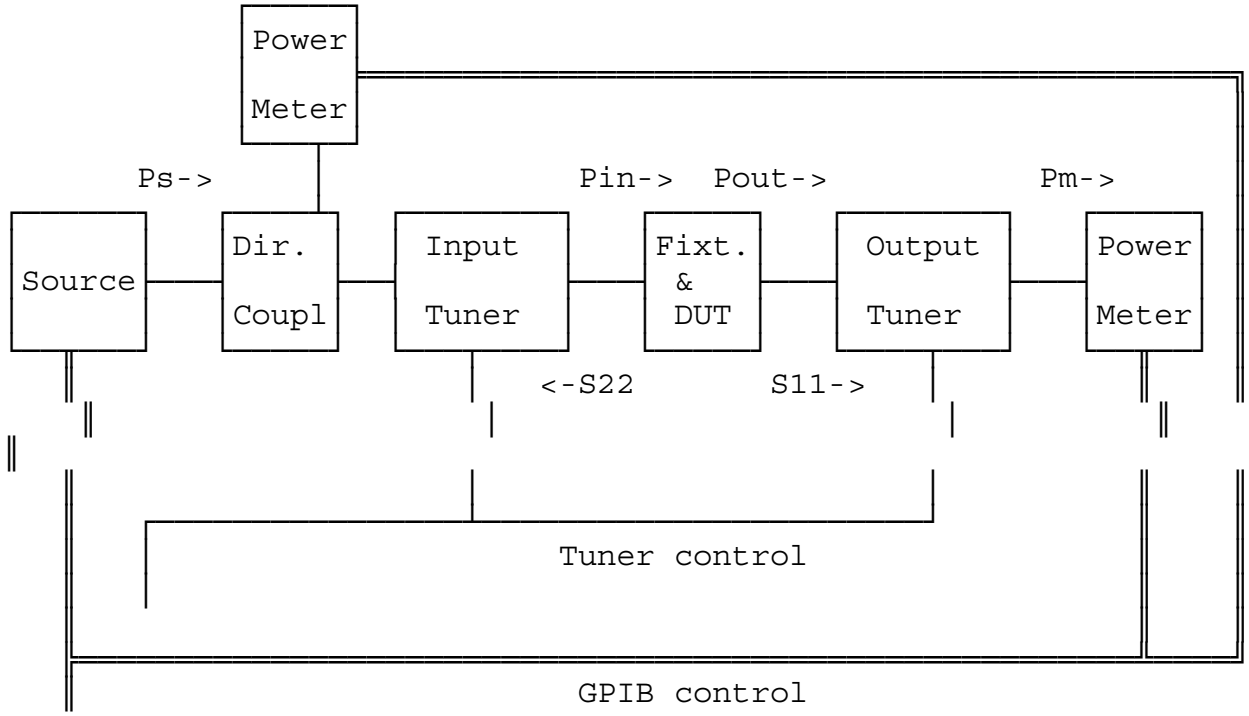


Figure 2: Load Pull setup for Design Verification (DVP).

The impedances presented by the tuners to the transistor's input and output port will be set equal to the impedances of the matching networks, known through S-parameters files generated by the linear or nonlinear simulation software (Touchstone®, Compact®, MMICAD®, µW-PADS®, Libra®, MDS® or other...).
Since the losses of the networks computed by those software packages, however, will normally be different from the losses of the tuners, an adjustment (in addition to normal de-embedding to the DUT reference plane) is required.

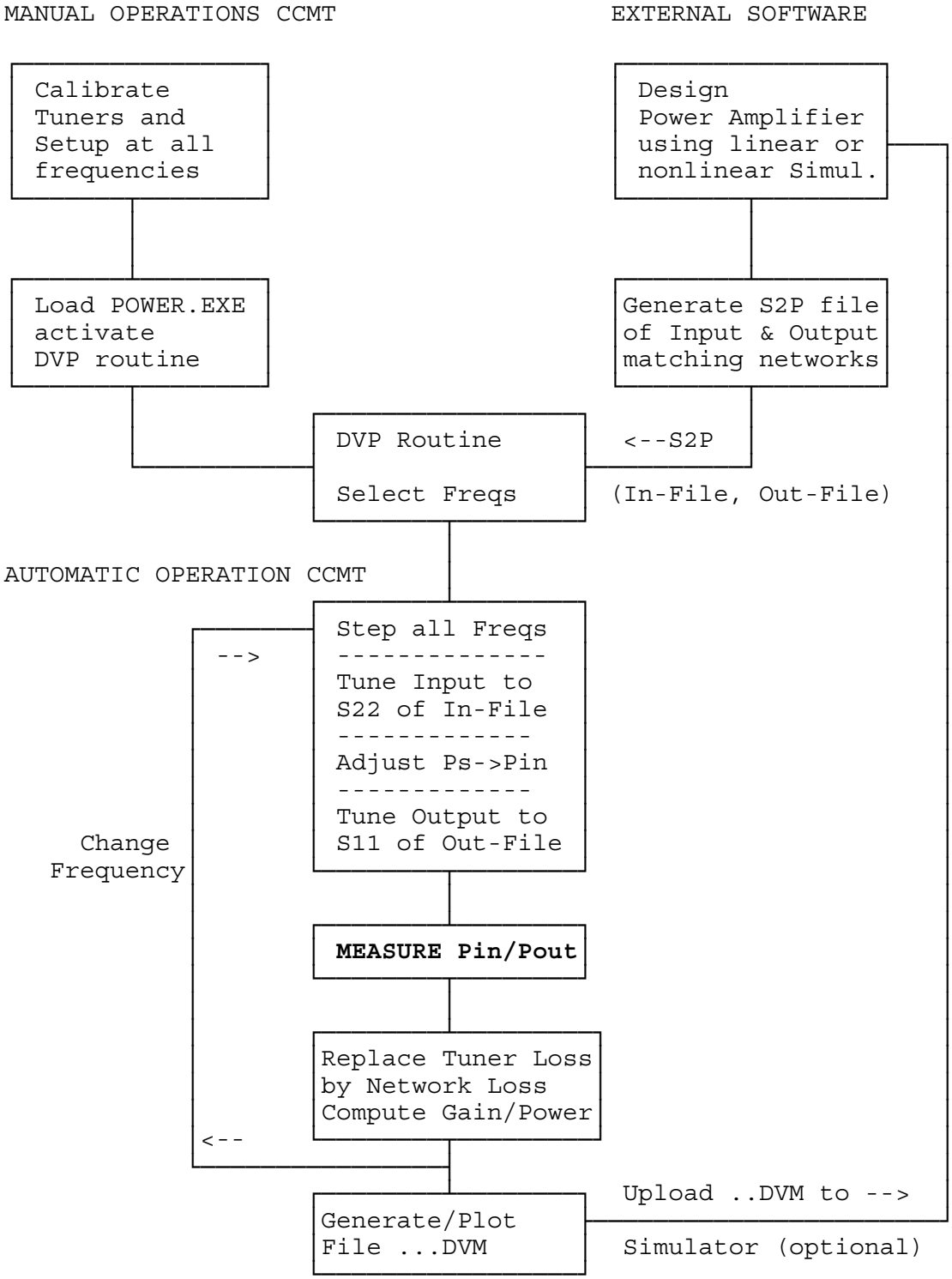
This adjustment consists of two actions:

1- Adjust the source power (Ps) such that the power actually available at the device's input (Pin) will be the same in test as in the actual amplifier.
2- Replace the losses of the tuners by the losses of the matching networks in order to display a 'corrected' measurement result.

Under these conditions a direct comparison between the measured gain by the load pull setup and the future amplifier is possible.

Design Verification Step by Step

The following is a flow chart of the Design Verification Procedure. The external software operations can be carried through using any of the commercially available network analysis and optimization software packages.



Example of Design Verification

Example of S2P type file (generated by external simulator) compatible with DVP. These files use the extension .CKI (for Input) and .CKO (for Output) for simple recognition by DVP.

```
! CKT-FILE: FLC3742.CKT
! NETWORK:  INPUT   (Tuner tunes to S22)
! CNT-FILE: FLC3742.CNT
!FREQ      S11            S12            S21            S22
!       MAG    ANG   MAG    ANG   MAG    ANG   MAG    ANG

  3.70  0.767   59.1  0.627 -141.6  0.627 -141.6  0.775 -162.6
  3.80  0.775   51.8  0.616 -145.7  0.616 -145.7  0.784 -163.5
  3.90  0.784   44.2  0.604 -149.9  0.604 -149.9  0.793 -164.4
  4.00  0.793   36.5  0.591 -154.3  0.591 -154.3  0.802 -165.3
  4.10  0.802   28.5  0.577 -158.7  0.577 -158.7  0.812 -166.2
  4.20  0.812   20.4  0.562 -163.2  0.562 -163.2  0.823 -167.1
```

Example of Design Verification file (extension .DVM) made using a μW-PADS design.

```
CIRCUIT  VERIFICATION  DATA
-------------------------------------------
Circuit file = FLC3742.CKI / .CKO
Verification file = C:\CCMT\DATA\FLC3742.DVM
-----------------------------------------------------------------
 CKT-FILE: FLC3742.CKT
 NETWORK:  TOTAL
 CNT-FILE: FLC3742.CNT
 CONTOUR-LEVEL: 31.00dBm
-------------------------------------------------------------------------------------
COMMENT = Pinput=22.5dBm, FET FLC161 #8, bias=8V,360mA
-------------------------------------------------------------------------------------
Freq/GHz   Γ,φ (Load)  Γ,φ (Source) DESIGNMEASURE   VERIFY Power Gain
~-----------------------------------------------------------------------
-------------------------------------------
 3.70      0.512 -154.2,  0.777 -162.530.93   30.84          30.84     8.25
 3.80      0.524 -156.0,  0.788 -163.330.86   30.83          30.89     8.19
 3.90      0.536 -157.7,  0.799 -164.230.96   30.81          30.99     8.20
 4.00      0.547 -159.5,  0.807 -165.031.04   30.84          31.05     8.36
 4.10      0.559 -161.2,  0.815 -165.931.04   30.87          31.03     8.27
 4.20      0.571 -163.0,  0.824 -166.931.09   30.94          30.79     8.34
```

The four columns after the frequency show the reflection factors synthesized by the tuners. Column 6 (DESIGN) shows the predicted performance (in dBm). Column 8 shows the result of DVP (VERIFY) and column 7 (MEASURE) the performance of the **first iteration**. It is clear that if a design verifies as close to the predictions as this example, a **first pass operation** is certain or at least very probable.

Effect of Harmonic Loading

Design Verification is based on fundamental frequency data and tuning. The CCMT tuners (as any other passive tuner) do represent an impedance at the harmonic frequencies, but this cannot be controlled. The impedances presented by the tuners at the harmonic frequencies will also be different than the impedances of the passive circuits designed. At this point only some sophisticated feedback (active) load pull systems provide information about harmonic loading. If such a system can be used, then it must also be able to tune to all the harmonic impedances (as generated by the design) independently.
This approach, if properly implemented, will certainly improve the accuracy of a Multi Harmonic DVP.

However, the example shown above uses a transistor operating about 2-3 dB into gain compression. The results of the design and verification are so close to the measured data, that it can be suggested that harmonic loading is, at least in this and similar cases, insignificant. Further designs, using higher power FETs (45 dBm) showed similar agreement between Design-Verification and Measurement.

This confirms the assumption, that for practical purposes of high power amplifier designs DVP provides a useful tool of Design Verification, able to cut design cost by avoiding iteration failures.

Further Reading

[1] Design a power amplifier stage using µW-PADS, Technical Note 1-92, Focus Microwaves.
[2] A novel Design method for wideband power amplifiers, Microwave Journal, May 1992, page 303.
[3] CCMT-Operation Manual, section 4.10.5 (DVP).
[4] Load pull measurements on transistors with harmonic impedance control, Application Note no 11, Focus Microwaves.
[5] Ghannouchi et al. "A multi harmonic loading method for large signal microwave and millimetre-wave transistor characterization", IEEE-MTT, vol 39(1991),p 968ff
[6] Hughes et al. "Accurate on-wafer power and harmonic measurements...", MTT-S 1992, p. 1019ff