

On-Wafer Load Pull Characterization of W-Band InP HEMT Unit Cells for CPW MMIC Medium Power Amplifiers

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Abstract — A W-Band on-wafer, vector source and load pull system has been implemented and applied to the systematic determination of the optimum, large signal, input and output impedances of indium phosphide (InP) HEMT cells as a function of bias and high power RF drive. The large signal optimization of a variety of device styles and sizes, so as to achieve a 'priori' W-band power and gain goals, resulted in an optimal HEMT cell geometry and first pass design success of W-band, finite ground coplanar waveguide (FGCPW) medium power amplifiers. These state-of-the-art amplifiers employing single 150 μm and 250 μm device cells deliver output powers of 13.8 dBm and 16.7 dBm with efficiencies of 23% and 17.5%, respectively.

I. INTRODUCTION

The key to achieving optimum performance with any solid state transistor at millimeter-wave frequencies is creating a conjugate power match at the input and output of the device under large signal RF drive and bias conditions. Large signal device models have limited accuracy for the new W-band device architectures. Experimental, on-wafer, W-band characterization is preferable and feasibility has been reported at W-band by Alekseev, et. al. [1]. Additionally, the authors have observed that the physical structure and layout of the device can provide radically different performance from devices with similar gate peripheries but different geometries, hence requiring careful design of the device structure.

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The authors have assembled and successfully implemented an on-wafer vector Source and Load pull system for characterizing InP-based HEMTs at W-band and developed a procedure to determine the optimum HEMT layout for best MMIC performance given a set of power amplifier performance goals. The system is calibrated to the terminals of the device and has been employed to characterize a variety of coplanar waveguide (CPW) InP HEMTs of various geometries so as to select the optimum layouts of HEMT unit cell power devices. The input and output matching data was subsequently used to achieve first pass design success of W-band, medium power, MMIC amplifiers with state-of-the-art performance for a finite ground CPW InP-based MMIC at this frequency. It should also be noted that these amplifiers were designed for specific performance goals and the resultant MMICs did not require external tuning but operated into a 50 ohm load impedance. This performance verified the accuracy of the large signal input and output impedance data for the devices, which is critical for optimum matching network design.

II. ON-WAFER VECTOR LOAD PULL SYSTEM

The on-wafer W-band Source and Load pull system is based upon high-precision electromechanical computer controlled waveguide (WR-10) tuners and measurement software [2]. The tuners provide coverage of the Smith chart to a $|\Gamma| = 0.9$ at the tuner waveguide flange. A high power, 93 - 95 GHz, Gunn diode oscillator is used as the signal source for the system to insure that the devices encounter a variety of large signal RF operating conditions for a given bias during the measurement. An input coupler and circulator are configured to measure forward and reflected power. Minimization of the reflected signal insures high level RF drive to the device input and algorithms are employed to determine the optimum input matching impedance. An output coupler

on the load tuner output, measures the calibrated output power and is also used to monitor the downconverted frequency spectrum of the device after signal amplification. Observation of the output spectrum is necessary to insure that either in-band oscillations or spurious signals from the device are not present. Furthermore, instrumenting the bias lines of the device is necessary to search for low frequency oscillations, which can result in a degraded spectrum or device failure. The tuners and all waveguide components are mounted on 3-axis positioners on a wafer probe system. Low insertion loss Picoprobe [3] W-band wafer probes with built-in bias networks were attached to the device side of the tuners for on-wafer testing. The entire system is depicted in Figure 1.

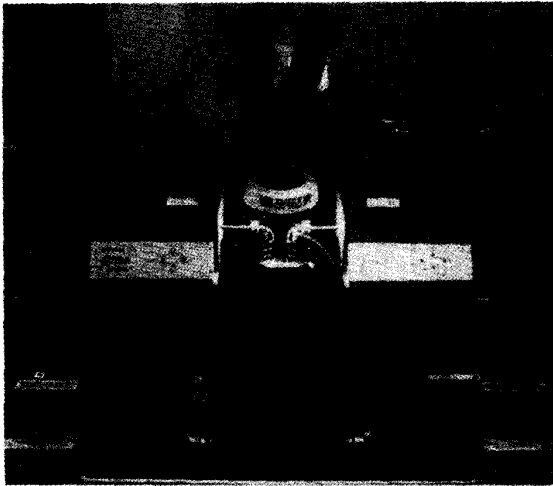


Figure 1. W-Band on-wafer vector source/load pull characterization station.

Accurate system calibration is crucial to achieving useful large signal device data. The calibration is accomplished in software by describing each portion of the network with S-parameters that are systematically stored in a file and later used to de-embed to the device terminals. The S-parameters of the tuners are measured for a variety of tuner position settings so as to encompass the entire Smith Chart. Both the tuner and the other waveguide subassemblies are measured over the desired W-band frequency range and step increment using an HP 8510B/C Vector Network Analyzer with W-band option. The low loss wafer probes were characterized with a Thru-Reflect-Line (TRL) calibration procedure developed by Herman [4]. Herman demonstrated the accuracy of his calibration procedure at millimeter-wave frequencies.

The TRL standards [4,5,6] used to calibrate the probes were manufactured on the same InP wafer containing the device cells of interest. This approach eliminates any variability in the calibration parameters that might be encountered from calibrating on a substrate standard different from the InP wafer. The vector network analyzer data of the probes is processed through a PC-compatible FORTRAN code [7], based on Herman's aforementioned TRL procedure, to extract the S-parameters for each probe as well as a portion of the wafer thru standard. The test devices are manufactured on the wafer to include half of the thru standard on the input and output of the device to maintain the reference plane directly at the gate and drain of each HEMT cell during the measurements. This process insures accurate large signal input and output impedance data.

III. InP HEMT UNIT CELL EVALUATIONS

Multiple device configurations from a 0.1 μm InP HEMT process were characterized using the load pull station. Combinations of three multiples (2, 4, and 6) of four different gate finger widths (25, 37.5, 41.7 and 50 μm) in parallel resulted in seven different total gate peripheries (50, 75, 100, 150, 200, 225 and 250 μm) for the HEMT unit cell. For each device, several measurements were made under different bias conditions and frequencies to determine the optimum bias conditions for that particular HEMT periphery. A typical data plot showing the output power contour data for a 4 x 37.5 μm HEMT at 95 GHz is shown in Figure 2.

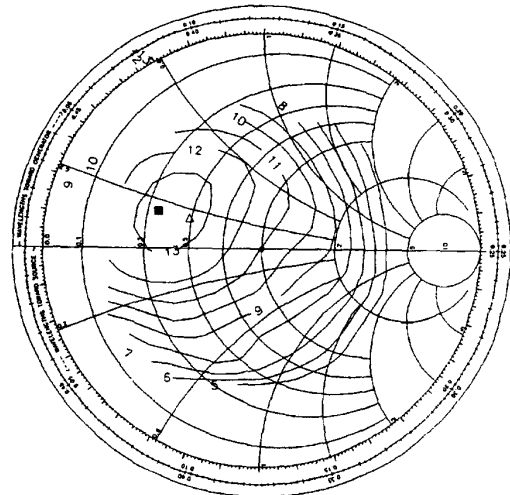


Figure 2. Load pull contours for a 4 x 37.5 μm HEMT at 95 GHz.

As more gate fingers are placed in parallel, the effect on the output load impedance is similar to placing resistors in parallel. The loss of the wafer probes limits the maximum reflection that can be presented at the device terminals, resulting in a limited tuning range that will not adequately close the contours of larger periphery devices ($>150 \mu\text{m}$ gate periphery). Characterizing the movement of the optimum large signal, matching load impedance as a function of gate finger count for a given gate finger size can be used to effectively estimate the optimum load for these larger devices. For example, the large signal load impedance change for different multiples (2, 4, and 6) of the same gate finger width ($25 \mu\text{m}$) are illustrated in Figure 3. In this case, the $6 \times 25 \text{ mm}$ device has a small enough periphery that the contours were nearly closed, but with larger gate finger sizes (i.e. $37.5 \mu\text{m}$ or $41.7 \mu\text{m}$) the contours would be relatively flat at the edge of the tuning range. An approximation of optimum load impedance can be made using the contour data for the angle and the device scaling data for the magnitude.

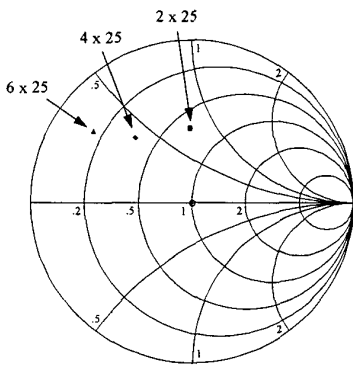


Figure 3. Load pull measured peak performance impedances at 94 GHz for $50 \mu\text{m}$, $100 \mu\text{m}$ and $150 \mu\text{m}$ InP HEMT unit cells.

IV. MMIC DESIGN AND LARGER PERIPHERY DEVICE CHARACTERIZATION

The load pull data from the InP HEMT unit cell characterization was used to select an optimum HEMT unit cell and design two single-stage single-ended MMIC MPAs, reported elsewhere [8], in finite-ground CPW using a $150 \mu\text{m}$ ($4 \times 37.5 \mu\text{m}$) and $250 \mu\text{m}$ ($6 \times 41.7 \mu\text{m}$) HEMT. The performance of these MMIC amplifiers, repeated here for convenience in Figures 4 and 5, indicates first pass design success using the HEMT unit cell load pull characterization data.

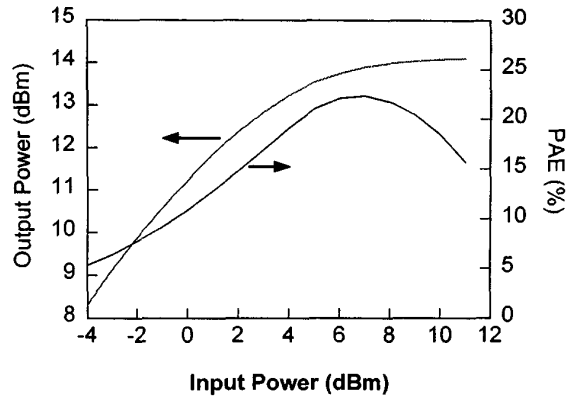


Figure 4. Measured output power and efficiency at 94 GHz of a single-stage coplanar amplifier MMIC using a $150 \mu\text{m}$ InP HEMT unit cell.

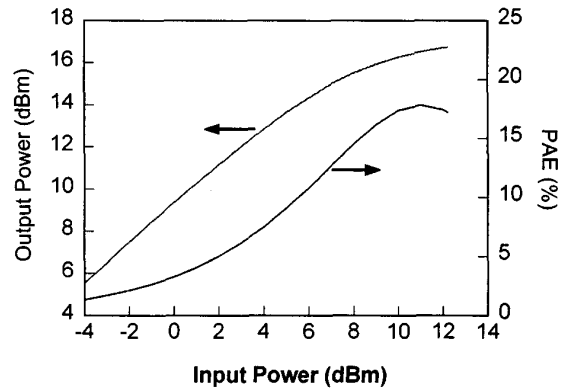


Figure 5. Measured output power and efficiency at 94 GHz of a single-stage coplanar amplifier MMIC using a $250 \mu\text{m}$ InP HEMT unit cell.

To attempt direct measurement of some of the larger periphery devices, on-wafer, quarter-wave, CPW impedance transformers were constructed on a subsequent MMIC wafer run to shift the tuning range toward the desired impedances [9]. Load pull contours for a $250 \mu\text{m}$ device using the transformers are shown in Figure 6. Note that for proper spacing of the measured points, the Smith chart in Figure 6 is re-normalized to 30Ω . Although the contours in Figure 6 are not completely closed, the contours are much more rounded than the data for a similar sized HEMT without the transformer. The optimum load impedance is consistent with the approximated impedance without the transformer and substantiated the matching impedance used in the amplifier design. Additionally, the peak performance point indicated in the load pull data is a output power of

16.6 dBm which is close to the measured performance of the MMIC amp.

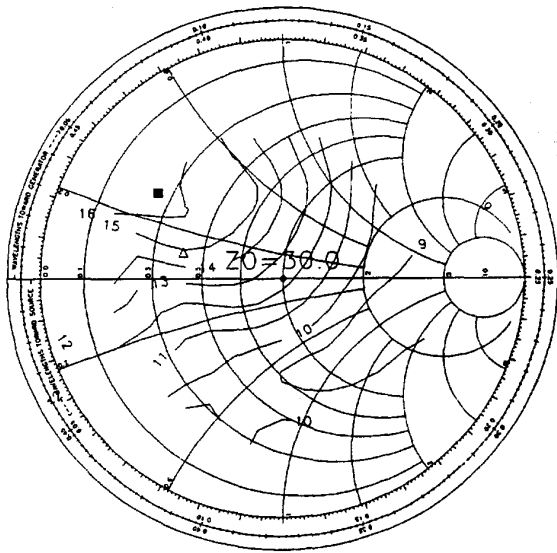


Figure 6. Load pull contours of a pre-matched 250 μm HEMT unit cell. The Smith chart has been re-normalized to 30 Ω .

V. CONCLUSIONS

An on-wafer W-band, vector, source and load pull measurement system has been assembled and used to characterize InP-based CPW HEMTs. Various device geometries were characterized for impedance match and saturation characteristics using the station. This data allowed selection of a gate finger structure that provided optimum performance for a given gate periphery for a set of power and gain design goals. Single-ended single-stage finite-ground CPW MMICs were designed and fabricated using two different gate peripheries that performed well in the load pull characterization. Subsequent, source data also facilitated the design of the multi-stage FGCPW amplifiers. The HEMT unit cell characterization procedure described here was critical to the first-pass design success of the fabricated MMIC MPAs with state-of-the-art performance.

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