

# High Power Performance InP/InGaAs Single HBTs

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**Abstract.** In this study, single- and multiple-finger HBTs were fabricated from epilayers grown in-house by low-pressure metal organic vapor phase epitaxy (LP-MOVPE). Disilane and DEZn were used for Si and Zn sources for *n*- and *p*-type doping. The gas switching sequences were optimized for optimal layers and layer interfaces. The HBTs were fabricated with a double self-aligned wet-etch process designed for reduced device parasitics. Base contacts were Pt/Ti/Pt/Au, which gave a contact resistivity as low as  $1.3 \times 10^{-6} \Omega \cdot \text{cm}^2$ . High-frequency performance for  $1 \times 10\text{-}\mu\text{m}^2$  emitter HBTs was 93 GHz and 67 GHz for  $f_T$  and  $f_{max}$ , respectively. DC current densities were as high as  $1.4 \times 10^5 \text{ A/cm}^2$ . Power and load-pull measurements were carried out at 10 GHz to determine device performance at optimal matching conditions. The maximum power density achieved was  $1.37 \text{ mW}/\mu\text{m}^2$  for an HBT with a 4-finger ( $2 \times 10 \mu\text{m}$  each) emitter. The maximum output power obtained was 22.58 dBm for a larger device (4 fingers of  $5 \times 10 \mu\text{m}$  each). These characteristics demonstrate good power driving capability for unthinned single HBTs which employ a simple InGaAs collector design.

## 1. Introduction

InP/InGaAs HBTs offer a number of advantages over AlGaAs/GaAs HBTs resulting from the inherent properties of the InP-based material system. Results up to now on InP/InGaAs single HBTs, however, emphasized primarily high-frequency operation characteristics [1], and only little has been reported on their power performance due to their relatively low breakdown voltages imposed by the low bandgap InGaAs collector [2]. Recent data on power performance of InP-based HBTs have primarily focused on InP/InGaAs/InP or InAlAs/InGaAs/InP double HBTs since their InP collector offers the possibility of higher breakdown voltages [3]. However, the conduction band spike at the base-collector heterojunction of double HBTs tends to degrade the electron transport and subsequently the high speed performance of the device unless special collector designs are used [4]. This paper addresses the design, growth, and fabrication technology of single HBTs with InGaAs collectors and demonstrates good high-frequency and high-power characteristics for such devices.

## 2. MOVPE growth of InP/InGaAs HBTs

The InP/InGaAs HBTs presented in this work were grown by a modified EMCORE GS3200 low-pressure metal organic vapor phase epitaxy (LP-MOVPE) system at the University of Michigan. Trimethylindium (TMIn) and trimethylgallium (TMGa) were used for In and Ga sources, respectively, and 100% arsine ( $\text{AsH}_3$ ) and phosphine ( $\text{PH}_3$ ) were used for group V sources. The *n*-type dopant was 1% disilane ( $\text{Si}_2\text{H}_6$ ) diluted in hydrogen and controlled by double-dilution lines capable of controlling the dopant flux with a dynamic range over  $10^4$ . The *p*-type dopant was diethylzinc (DEZn). The susceptor rotation was fixed at a low value of 100 rpm since this offered best thickness and compositional uniformity across the wafer, as well as higher source incorporation efficiencies [5].

All layers were grown on an Fe-doped semi-insulating InP substrate with exact (100) surface. The layer structure used for the HBTs in this study is as follows: 1000 Å undoped InP buffer, 5000 Å  $n^+$  InGaAs subcollector, 5000 Å  $n^-$  InGaAs collector, 600 Å  $p^+$  InGaAs base, 100 Å undoped InGaAs spacer, 1500 Å  $n^-$  InP emitter, 700 Å  $n^+$  InP contact layer, and 2000 Å  $n^+$  InGaAs cap. The base doping was approximately  $1.5 \times 10^{19} \text{ cm}^{-3}$ .

Gas switching sequences for normal and inverted InP/InGaAs heterointerfaces were optimized to avoid quaternary formation at the interfaces. The growth cycle employed for this purpose included a transition from InGaAs to InP by (i) switching off the TMI<sub>n</sub> and TMGa followed by 5 seconds of purging, (ii) exchanging the group V source from AsH<sub>3</sub> to PH<sub>3</sub> with 1 second overlap and (iii) 10 seconds of purging time before introducing TMI<sub>n</sub> for InP growth. The transition from InP to InGaAs was done following a similar procedure where InGaAs growth started immediately after the group V exchange. This allowed consistent and controlled selective etching during device fabrication since no ternary residuals were formed and led to improved device performance.

In order to minimize zinc diffusion from the heavily zinc-doped base to the emitter, sufficient gas purging time was provided after growing the InGaAs base in conjunction with a 100-Å undoped InGaAs spacer. Silicon encroachment from the heavily-doped subcollector to the lightly-doped collector layer was minimized by purging the dopant dilution line between the two layers. By precisely controlling the dopant profile in the collector regions, the full width of the depletion region was maintained, which greatly improved breakdown characteristics of the devices.

### 3. Technology of InP/InGaAs HBTs

The devices analyzed in this paper were fabricated using double self-aligned technology with an all wet etching process. After deposition of the emitter ohmic contact (Ti/Pt/Au), the wafer was etched down to the base layer by repeated selective wet etches of the emitter cap, emitter, and spacer layers. The base metal, Pt/Ti/Pt/Au, was deposited self-aligned along two parallel edges of the emitter finger, such that the emitter undercut profile under the emitter metal was identical under all self-aligned edges. The emitter etching times were carefully designed to reliably obtain an emitter undercut so that the lateral distance from the self-aligned base metal to the emitter semiconductor was 0.2-μm. After base deposition, the contacts were annealed at 375° C for 7 seconds, which stabilized the base contacts and lowered their contact resistivities to  $1.3 \times 10^{-6} \Omega \cdot \text{cm}^2$ .

In order to reduce extrinsic base-collector junction capacitances, the emitter fingers were protected with photoresist patterns while the base semiconductor layer was etched away self-aligned to the base metal contacts. This step effectively reduced the semiconductor junction areas to those directly under the emitter and base metalizations. After the Ti/Pt/Au collector was patterned and lifted off, the HBTs were isolated from one another to the semi-insulating InP level through a wet etch. The same wet etch was used to form trenches in the semiconductor under the emitter and base metalizations, which isolated the semiconductor in the intrinsic device areas from the semiconductor under the airbridge contact pads. The junctions under the airbridge pads are therefore isolated and do not contribute to parasitic capacitances ( $C_{be}$  and  $C_{bc}$ ). Finally, gold airbridges were electroplated to connect the HBTs to interconnects and coplanar testing pads.

The HBTs that were fabricated were all variations on two basic designs: a high-frequency device with thin ( $2 \times 10 \mu\text{m}^2$ ) emitter fingers and trench-isolated pads for airbridge contacts, and a high-power device with wide ( $5 \times 10 \mu\text{m}^2$ ) emitter fingers which were directly contacted by the emitter airbridge. Variations on the basic devices were fabricated, including multifinger HBTs. A plan-view photograph of a 10-finger HBT is shown in *Figure 1*.



**Figure 1:** Photo of HBT in common-emitter configuration with 10 fingers, each  $2 \times 20 \mu\text{m}^2$ . Electroplated gold forms the airbridge interconnections, soft contact pads of coplanar microwave probes, and heat sinking.

### 4. DC and small-signal microwave characterization

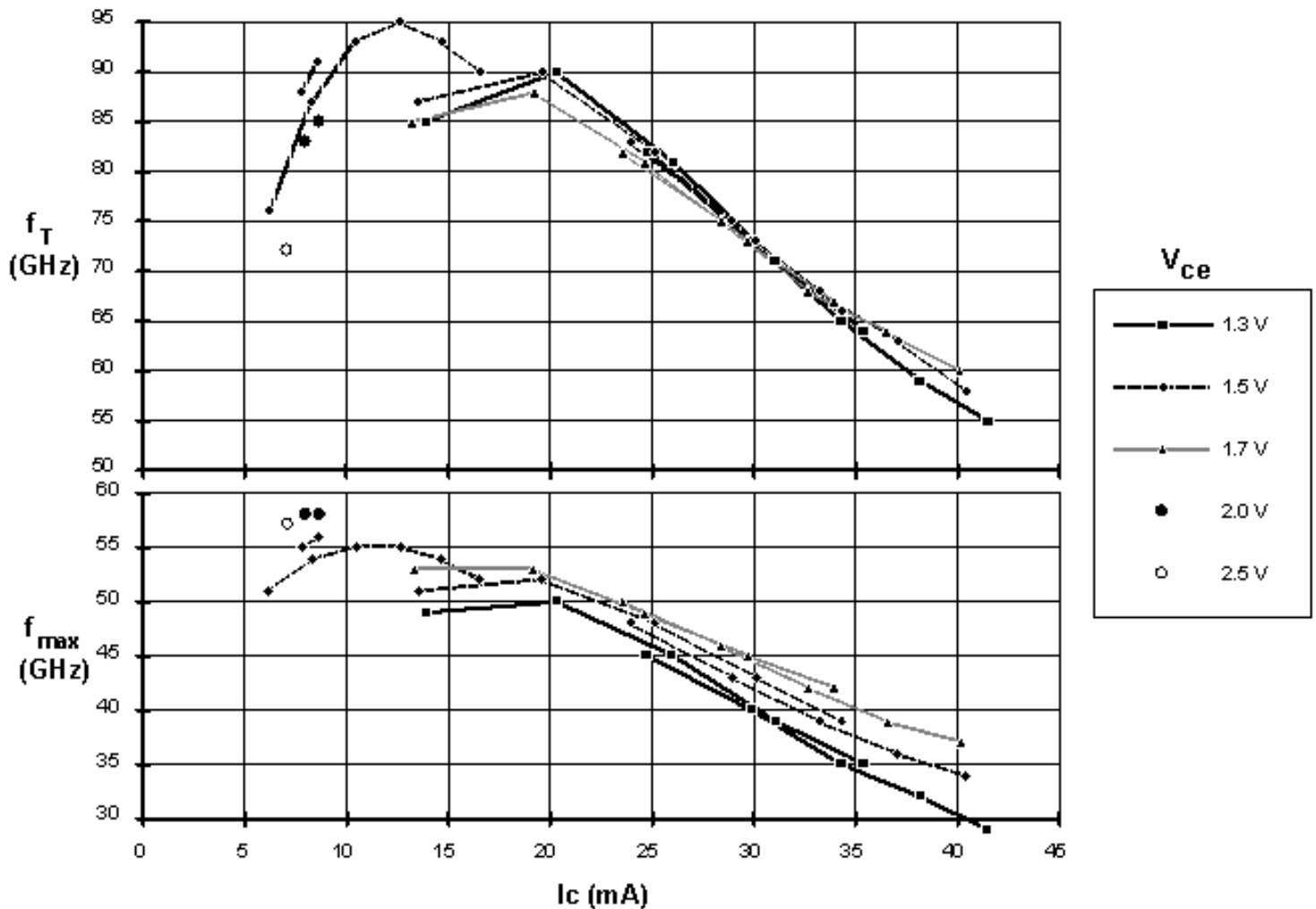
The DC characteristics of the fabricated devices proved to be good for single InP/InGaAs HBTs. Breakdown voltages

for large devices were as high as  $BV_{ce} = 7.2$  V at  $I_c = 10$  mA. Maximum collector current densities were also high and about  $J_c = 1.4 \times 10^5$  A/cm<sup>2</sup>. The common-emitter I-V plot for a  $5 \times 10 \mu\text{m}^2$  HBT is shown in Figure 2. The collector- and base-current ideality factors from forward Gummel plots were  $n_c = 1.3$  and  $n_b = 1.4$ , respectively, for the same device.



**Figure 2:** Forward common-emitter I-V plot of HBT with  $5 \times 10 \mu\text{m}^2$  emitter.  $I_b = 0.1$  mA/step.

The microwave characteristics were measured on a HP 8510 network analyzer up to 25.5 GHz. Measurements from  $|h_{21}|^2$  and  $U$  were extrapolated at 20 dB/decade to find  $f_T$  and  $f_{max}$ , respectively. While showing good breakdown characteristics, these devices also showed good high frequency performance. Maximum values of  $f_T$  and  $f_{max}$  for  $1 \times 10 \mu\text{m}^2$ ,  $2 \times 10 \mu\text{m}^2$ , and  $5 \times 10 \mu\text{m}^2$  emitters, respectively, were 93 and 67 GHz, 95 and 55 GHz, and 97 and 51 GHz. The degradation of  $f_{max}$  with increasing device size indicates that  $f_{max}$  is dominated by the  $R_b C_{bc}$  time constant. Variations of  $f_T$  and  $f_{max}$  with respect to bias for a  $2 \times 10 \mu\text{m}^2$  HBT are shown in Figure 3. The drop in performance at high current levels is likely to be due to base push-out and heating effects. A small-signal equivalent circuit [6] was fitted to the  $2 \times 10 \mu\text{m}^2$  HBT at  $I_c = 12.6$  mA and  $V_{ce} = 1.5$  V, giving  $R_b = 9.8 \Omega$ ,  $C_{bc} = 34$  fF, and  $\tau_b + \tau_{pcd} \approx 0.6$  ps. The equivalent circuit indicates that the total delay time ( $\tau_{ec} = 1 / 2\pi f_T = 1.7$  ps) is also dominated by RC charging time constants.

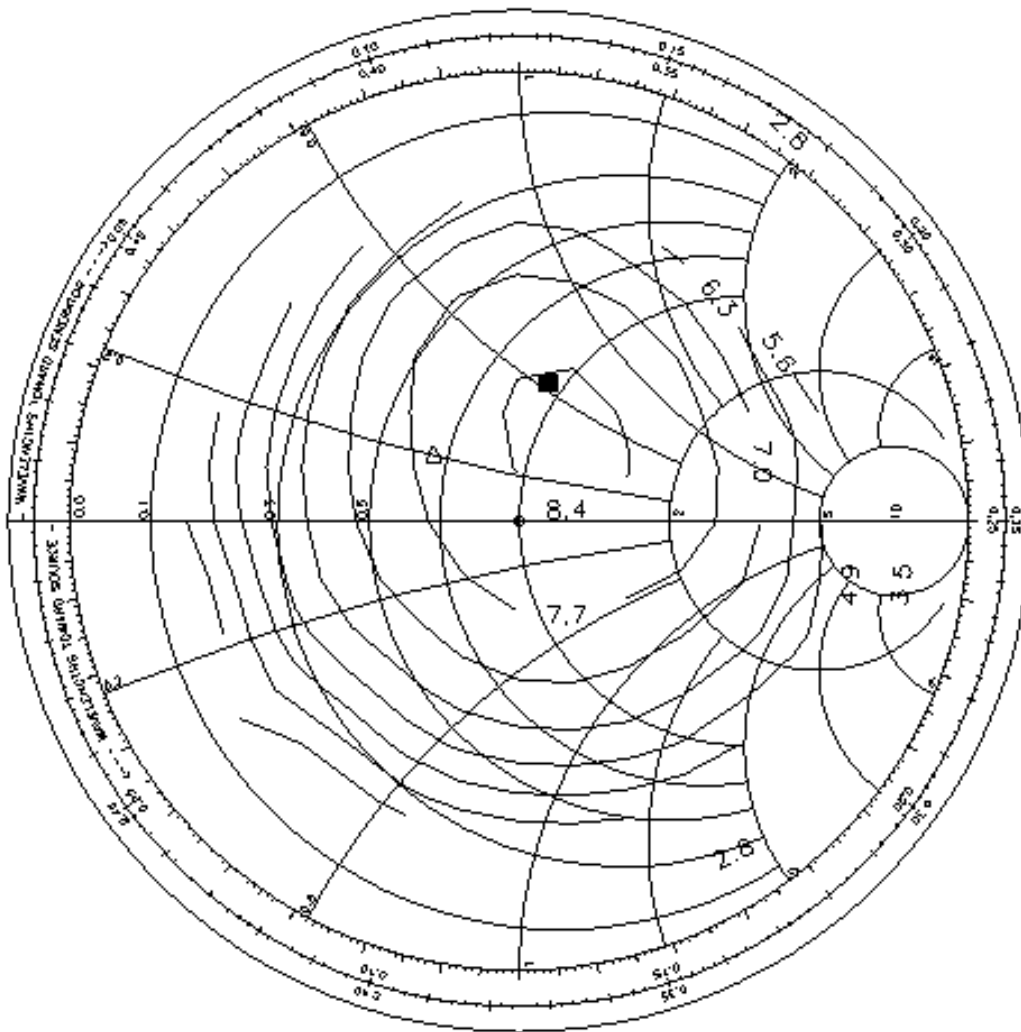


**Figure 3:** Dependence of  $f_T$  and  $f_{max}$  on DC bias of a  $2 \times 10\text{-}\mu\text{m}^2$  HBT. Four identical HBTs were measured, two at low current densities and two at high current densities.

## 5. Large-signal power characterization

The HBTs characterized for power performance in this work had emitter areas of  $4f \times (5 \times 10)\ \mu\text{m}^2$ ,  $4f \times (2 \times 10)\ \mu\text{m}^2$ , and  $1f \times (5 \times 10)\ \mu\text{m}^2$ . Load-pull measurements were carried out on-wafer using [electromechanical tuners](#) in an in-house developed setup. This allowed on-wafer large-signal HBT characterization at the device level and thus extraction of device characteristics under conditions of reduced parasitics. All three transistors were tested at 10 GHz and at a variety of available input power levels and loading conditions.

The dependence of the output power contours on load termination for the  $1f \times (5 \times 10)\ \mu\text{m}^2$  device is illustrated in *Figure 4* for input power  $P_{in} = -1.05\ \text{dBm}$ . The maximum gain is 9.6 dB at  $Z_L = 46.4 + j32.8\ \Omega$ . At lower input power levels, the contours of constant output power were qualitatively quite similar but at lower output power levels. At higher input power levels, the contours of constant output power distorted into ellipses, and the load impedance giving maximum gain shifted closer towards the center. The variation of the shape of these contours was a result of the nonlinearities/gain compression characteristics of HBT at high power levels.



**Figure 4:** Constant load-pull output power contours of  $1f \times (5 \times 10)\ \mu\text{m}^2$  HBT at  $P_{in} = -1.05\ \text{dBm}$  and  $f = 10\ \text{GHz}$ . Values are in dBm.

The loading conditions at both the input and output of the transistor resulting in maximum output power were evaluated as a function of the power level exciting the device. This allowed for determination of the conditions that provide maximum gain at small-signal power levels as well as those that yield maximum power at larger power levels. To exploit the maximum output power capabilities of all three devices used in this study, a special software routine was employed for controlling the automated tuner system. This routine searched for the termination conditions at a particular input power that resulted in maximum gain and output power. Thus the characterization approach of this work consisted of searching for such conditions at very high power levels for each of the transistors. In this way, the capabilities for maximum power delivery of the devices were analyzed.

Another condition that assured maximum output power delivery was to employ a constant  $V_{be}$  in order to bias the base-emitter junction. This allowed the emitter-base junction to stay on at high power levels and led the transistor to high collector current and, consequently, to high output power operation. This also forces Class A operation, however, which limits the power added efficiency of the devices.

The main factor limiting high power performance of single InP/InGaAs HBTs is the use of low  $V_{ce}$  values due to the usually low breakdown voltages exhibited by such devices. In the case of our transistors, the breakdown behavior was improved by using 5000-Å collector layers. Another prerequisite ensuring high power driving capabilities is the potential for high output current operation. This was ensured in this work by the design of multi-emitter finger HBTs.

Measurements were carried out at collector current levels between 10 and 200 mA and  $V_{ce} = 2$  V. *Figure 5* shows the output versus input power characteristics for all three transistors. As one observes, the two smaller devices showed a higher small-signal gain of 10 dB versus 5 dB gain of the  $4f \times (5 \times 10) \mu\text{m}^2$  device at  $P_{in} = 0$  dBm. This is attributed to the higher base-collector capacitance of the latter device.

**Figure 5:** Comparison of power driving capability of HBTs with varying geometries at 10 GHz.

Moreover, the smallest device in emitter size shows lowest output power driving capabilities. In contrary, the largest device in emitter area shows a maximum output power of 22.58 dBm corresponding to a density of  $0.9 \text{ mW}/\mu\text{m}^2$ . This is attributed to the higher current driving capabilities of this transistor compared to the other two devices. On the other hand, the  $4f \times (2 \times 10) \mu\text{m}^2$  emitter area device showed best output power density of  $1.37 \text{ mW}/\mu\text{m}^2$ . Furthermore, a maximum power added efficiency of 33.9% was measured for this transistor, which also is best among the three devices studied in this work. The power density of  $1.37 \text{ mW}/\mu\text{m}^2$  obtained from the four-finger device demonstrates very promising characteristics from unthinned single InP/InGaAs HBTs on 370- $\mu\text{m}$  thick InP substrates.

*Figure 6* shows the dependence of self-biasing effects of the collector current on input power. As expected, the largest emitter area HBT shows maximum current driving capabilities. Moreover, these results indicate significant excursions from the nominal values of DC bias selected for HBT operation and provide further support of their good power driving capability.

**Figure 6:** Comparison of current driving capability of HBTs with varying geometries at 10 GHz.

## 6. Conclusion

InP/InGaAs HBTs were fabricated and their power characteristics were evaluated. The studies presented in this paper

provide a better insight to the power handling capabilities of InP-based single HBTs, which have not been addressed adequately in the past due to their typically low breakdown voltages. The HBTs were grown in-house by LP-MOVPE and fabricated using a double self-aligned process. Both their small- and large-signal performance was good for InP-based single HBTs, indicating excellent material growth and processing. While still a dominating factor,  $C_{bc}$  was significantly reduced through self-aligned etching of the extrinsic base semiconductor and through a special technology involving trench etches to isolate airbridge pads. This allowed for good high-frequency performance of  $f_T = 93$  GHz and  $f_{max} = 67$  GHz from  $1 \times 10 \mu\text{m}^2$  devices.

Good power performance was demonstrated from the InP/InGaAs HBTs by proper input and output matching selection, which was accurately controlled by means of large-signal on-wafer probing. Breakdown voltages of 7.2 V were demonstrated at 10  $\mu\text{A}$ . Output power densities as high as 1.37 mW/ $\mu\text{m}^2$  were achieved using  $4f \times (2 \times 10) \mu\text{m}^2$  emitter area devices. Moreover, multifinger HBTs were successfully implemented in InP-based HBT technology to increase the total output power handling.

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[\[GaN\]](#) [\[InP\]](#) [\[GaAs\]](#) [\[MOCVD\]](#) [\[Mixer\]](#) [\[Gunn \(NDR\)\]](#) [\[PIN\]](#) [\[HBTs\]](#) [\[HEMTs\]](#) [\[MMICs\]](#)

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