Designing Multi-Stage Class C Amplifiers for Pulsed Radar Applications

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Abstract

This paper describes a procedure for designing pulsed solid-state amplifiers for radar systems. Solid-state radar systems can be broadly divided into those using phase array antennas, and those using conventional, mechanically steered antennas.

Solid-state phased array radars (PAR's) generally distribute common transmit / receive (T/R) modules across a mechanical assembly that supports individual antennas. In some cases, T/R modules and antennas are integrated into a single assembly that attaches to a mechanical structure. Some systems have a mechanical structure that supports antennas, and signals connect from T/R modules to antennas through transmission lines (i.e. coax or waveguide). In either case, modules are mechanically distributed across the array, and are electronically adjusted in phase to steer the radar beam.

Transmitters in conventional solid-state radar systems combine power from a large number of modules, often using radial combiners. Modules are assembled in cabinets that have a single, high power output connector that feeds a T/R switch and/or other common circuitry (e.g. filter, circulator, etc.). The system connects to a mechanically steered antenna.

RF transmitter power in both types of systems is generated by a large number of common amplifiers. The procedure described in this paper is suitable for designing amplifiers used in either system.

Key words:- RF Power Amplifier, Pulsed Amplifier, Radar Amplifier, T/R Module

Introduction

An amplifier design starts by reviewing its specification for overall performance. Requirements are compared to performance of available components to develop an architecture, determine performance of individual stages, and loss of passive components. A spreadsheet or similar tool projects performance of the overall assembly. Spreadsheet results lead to a block diagram that shows the amplifier's architecture and lists performance of individual stages and passive components. A successful design results when overall specifications realistically represent performance that can be achieved using available components. Performance, reliability and cost are all important aspects of a design. While all three are discussed, the focus of this paper is electrical performance.

This paper is illustrated by a typical three stage, S-Band, class C transmit amplifier design. The example could be used as the RF Power Amplifier (RF-PA) subsection of a T/R module in a Phased Array Radar system, or as one of many RF-PA modules in a Conventional Radar system.

Performance Goals

When reviewing overall requirements, its important to identify how each parameter will be achieved. Often, some requirements cannot be met, or meeting them significantly increases cost and complexity. Parameters that are difficult or impossible to meet must be identified to see whether changes at the system level are needed to make the design practical. It is important to have design margin. If a paper design just meets the requirements, it may be impossible to consistently meet them in production.

Table 1, Proposed S-Band Amplifier Performance Goals

Parameter	Requirement
Frequency	3.1 to 3.4 GHz
Power Out	350 Watts
Pulse Width	100 uS
Duty	10%
Tr/Tf	< 100 nS
Gain	20 dB
Efficiency	27.5%
Insertion Phase	+/- 20º
VSWR stability	1.5:1
VSWR ruggedness	3:1
Voltage	36 V
T(operate)	-20 to +50C
T(storage)	-40 to +100C

It is important to know whether performance is specified for "room temperature" and allowed to vary over temperature within normal limits; or performance is

minimum over temperature. For this example, performance is specified at room temperature with normal variation permitted over temperature. This will be discussed later.

Reviewing the requirements in Table 1, bipolar transistors are available that operate over the specified frequency and under the specified pulse conditions. Available transistors produce approximately 100 Watts. It takes the combined output of at least 4 transistors to meet the module's output power requirement. Transistors in this frequency range have approximately 8 dB gain. At least 3 cascaded stages are needed to meet the overall gain requirement. It is good practice to protect the output of solid state amplifiers with an isolator (terminated circulator). This both protects the amplifier from mismatch, and isolates it from signals coupled to a module's output that might affect performance. Isolators add loss as well as cost, but generally, benefits outweigh both.

Three cascaded stages exceed the gain requirement, so some attenuation is needed. This has benefits:

By adjusting attenuation, gain can be set to meet overall performance and compensate for unit-to-unit variation.

Interstage loss improves stability.

Loss, however, reduces efficiency, and attenuators add cost. Again, benefits generally outweigh cost. It is best to minimize loss in output stages to maximize efficiency. Working from the output toward the input of an amplifier, once cumulative gain exceeds 10 to 15 dB, small additional losses have little effect on overall efficiency.

Stages are cascaded to increase gain, and paralleled to increase power. Stages are usually cascaded by first matching them to a common impedance (e.g. 50 ohms), then connecting matched stages in series. Stages are paralleled by matching to a common impedance then using splitters and combiners. Splitters and combiners can be designed in many ways. It is good practice to combine power using quadrature hybrids. Quadratures have the property of directing reflected waves to an isolated port. They do this as long as the reflection is the same at each output port. In a 4-port quadrature (i.e. one driving two), the reflection coefficient looking into the quadrature is low, even when reflection coefficient of the output ports is high, provided both output port reflection coefficients are reasonably well matched. Refer to the literature on quadrature hybrids for more information.

There are many 2-way quadrature designs, and several are commercially available as components. 2^N stages can be combined by cascading "N" 2-way quadratures. This is often referred to as corporate combining because a block diagram looks like a corporate organization chart.

Performance Spreadsheet

Once module performance requirements are understood, a spreadsheet is constructed to predict overall amplifier performance. It does this by combining gain of active stages, loss of attenuators, splitters and combiners, and gain or loss of other circuits. At the same time, the spreadsheet calculates overall current consumption and amplifier efficiency. A typical spreadsheet is shown below.

Table 2, Amplifier Performance Spreadsheet

				IB3134M100			IB3134M70		IB3134M25		
Parameter	Pout	Isolator	Combiner	Q3	Splitter	Attenuator	Q2	Attenuator	Q1	Pin	Total
Gain/Loss (dB)		-0.25	-0.45	8	-0.25	0	7	-2.5	9		
Power (Watts)	350	350	371	411	65	69	69	14	24	3.1	
Number Transistors				4			1		1		
Pwr/Transistor (W)				103	16.3		69		24		
Efficiency				40%			40%		40%		27.7%
Ic (Amps)				28.6			4.8		1.7		35.1

This spreadsheet starts at the output and works toward the input. This is done because the output stage in high power amplifiers is often the most critical:

The output stage establishes the number of active devices needed to achieve output power. The designer selects the most critical active component first, and then uses its performance characteristics to specify preceding, less critical stages.

It determines power needed to drive the output stage. This allows selection of an optimum driver. Attenuation, when needed, is added toward the input when possible. As mentioned previously, moving loss toward the input improves overall efficiency and lowers cost.

The process of adding stages continues from output to input until required gain is met or exceeded.

The second row in the spreadsheet lists Gain or Loss of each component. Data is entered from the keyboard (i.e.

not calculated). The next row lists Power in Watts. The first cell (350 Watts) is entered from the keyboard. Other cells are calculated using values from the Gain/Loss row. This is followed by a row, entered from the keyboard, indicating number of parallel transistors per stage. Below this row is calculated input and output power of individual transistors. Then a row, entered from the keyboard, lists collector efficiency of each transistor. The bottom row shows calculated current for each stage. Finally, the right hand column shows calculated amplifier gain, efficiency and current.

Transistor characteristics are entered stage by stage, left to right. Component characteristics correspond to either datasheet or measured values. As each transistor stage is specified, its performance determines requirements for the preceding stage. Transistors selected for this design are standard parts from Integra Technologies. All are class C biased, common-base silicon bipolar transistors. These Integra transistors were designed for radar applications.

Design Assessment

After the spreadsheet is completed, projected performance is compared to the requirements. It appears the requirements can nearly be met. Since components are typically de-rated (i.e. performance specified is MINIMUM), a prototype will likely meet the requirements. It should be noted, however, that production variations might cause problems for this design. Areas of most concern are output power and overall efficiency. If the output transistors only produce 100 Watts, and combiner and isolator losses are as listed, output power will be below 350 Watts. Additionally, efficiency only marginally meets its requirement.

Some potential solutions:

Reduce the amplifier's output power requirement.

Design lower loss combiners and isolators.

Use more output transistors.

A system level solution is to reduce individual RFA requirements (e.g. lower output power), and then add modules to compensate. This is often a practical solution because it adds less overall components. RF power amplifiers must be designed around optimum use of available components. Systems should be scaled around practical amplifier designs.[1] This example assumes the spreadsheet's projected performance is adequate for the RF Power Amplifiers.

Once the output stage is set, driver stages can be determined. The immediate driver, Q2, could use the same transistor as the output stage. This requires about 1.5 dB interstage attenuation, but would maintain a common design for 5 circuits. An interstage attenuator at this point will reduce efficiency approximately 2%. Because system efficiency is important, the alternate approach of using an available 70-Watt driver transistor is a better choice. At lower levels where performance is not significantly affected, use of common components (circuits) is recommended, even when overall performance degrades slightly.

Finally, the input stage transistor is selected. By adding a 2.5 dB attenuator, an available 25W transistor can be used. The attenuator is beneficial because it improves interstage impedance match.

Once a line-up is identified, individual circuits, both passive and active, are designed in detail. This involves characterizing components so individual circuits can be correctly designed and optimized. Designers initially use information from datasheets to provide characterization. Datasheet characterization, however, should be a starting point. Every critical component should be characterized because performance depends on an amplifier's environment, and layout constraints. Characterization adds information about component performance under specific conditions (e.g. information about parasitics associated with a particular substrate material, ground system, etc.), and over environmental conditions not shown on most datasheets.

Active Stage Design

This section focuses on design of active stages. Other amplifier elements are only briefly discussed. All critical elements, however, must be characterized during the design process. For example, if an amplifier will use surface mounted quadrature hybrids, the selected component should be characterized using the configuration planned for the amplifier. Performance of surface mounted quadratures is affected by grounding, signal line routing. This is only an example showing areas needing characterization by appropriate methods (e.g. network analyzer measurements; time domain reflectometry, etc.).

The best method to characterize RF power transistors is called "load pull." This characterization is done by operating a transistor into various load impedances while recording performance. For example, a transistor can be driven by a pulsed RF source at a particular operating frequency while recording input and output power, collector current, pulse droop, and other

[1] Note that marginal efficiency and power were designed into this example to illustrate a common design problem. It is always important for designs to have performance margin.

important parameters. Once data and associated impedance points are determined, contours of constant power, constant efficiency, or other contours are plotted, usually on a Smith chart. Sets of contours (e.g. output power and efficiency) can be overlaid to select compromise "optimum operating points." The process is repeated at various frequencies across a band of interest. Frequencies are spaced close enough to capture trends across the band. For our application (3.1 to 3.4 GHz), data can be taken at three points initially. If the data produces consistent plots, characteristics can be extrapolated between measured frequencies. If plots appear inconsistent, closer spacing must be used (e.g. every 100 or 50 MHz). The load pull process can be automated using commercially available equipment[2]. A manual load pull system is described in the below.

Load Pull Characterization

Load pull characterization involves matching a transistor on a point-by-point basis using tuners, recording performance and impedance, then plotting contours of constant performance on the impedance plane. It is necessary to start by placing the transistor into a "pre-matching" circuit that presents a reasonable match[3]. This circuit must also break-apart (i.e. a characterization fixture) to measure impedance presented to the transistor by its collector matching network plus external tuner.

Load pull can be measured as follows:

A transistor is operated in its "break-apart circuit" terminated by an external turner. The tuner should present small load variations (e.g. less than 3:1 mismatch) that either optimally match, or present known mismatch, to the transistor.

Tuner positions are locked (or recorded), and then RF performance is recorded.

The output break-apart "pre-matching" circuit and tuner are connected to a probe circuit.[4] The probe circuit can consist of a 50-ohm transmission line that connects to the pre-matching circuit and allows impedance measurement using a network analyzer. Ideally, a 50-ohm probe line's width is equal to width of the transistor's collector lead. It helps to use low dielectric constant material for the 50-ohm "probe." The network analyzer's reference plane is calibrated to the position where the transistor's collector lead normally contacts the circuit.

Impedance is recorded.

Characterization can be semi-automated using low loss trough line tuners. First, a transistor is operated in a break-apart circuit terminated by a trough line tuner. Dielectric tuning slugs are set to fixed positions that produce known load impedances. Successive measurements are spaced 20 to 30 degrees apart. This yields 12 to 18 data points for each slug assuming they are moved through 360 degrees of phase. The number of points is expanded by using slugs having different mismatches (i.e. different dielectric materials). Impedance points, referenced to the transistor's collector, are plotted on a Smith Chart along with corresponding RF data. Points having similar performance are connected, or constant contours are extrapolated between data points. This manual system produces results similar to that provided by commercial load pull systems. Accuracy is operator dependent, and the process is somewhat time consuming. It is, however, a cost effective procedure that provides information needed to optimize transistor matching. Figure 1 illustrates impedance data and an associated table showing measured performance. Data was plotted and contours were hand drawn.

Regardless of method, once load pull data is available, optimum impedances are selected for each frequency. Selected impedances often compromise two or more performance parameters, often efficiency or peak power is compromised.

The next step is synthesizing a matching network that transforms the load (usually 50 ohms) to the desired collector impedance contour. Here again, designers compromise because it is not possible to simultaneously match optimum impedance at every frequency. Performance generally degrades as frequency increases, so designers often optimize match at the high end of a band, and allow mismatch at lower frequencies. Load pull data can be used to select the best compromise match at lower frequencies.

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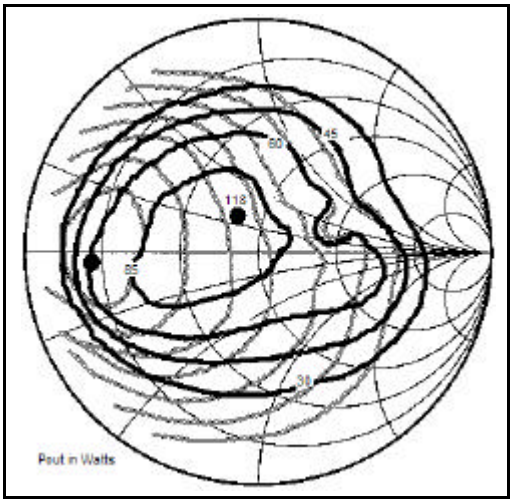
[2] See equipment manufactured by Maury Microwave (www.maurymicrowave.com) and Focus Microwave (www.focusmicrowave.com). Both web sites provide information on load pull and its use.

[3] If the pre-matching circuit is not close, losses will be high and it will not be possible to accurately measure TRANSISTOR performance. This is because loss will vary with load VSWR; measured performance results from transistor performance plus the varying (unknown) loss.

[4] By building two identical pre-matching circuits, the tuner can be moved from the transistor fixture to the second pre-matching circuit thereby avoiding removal of the transistor for impedance measurements.

Figure 1 – Load Pull Plot: Constant Power (labeled) & Efficiency (not labeled).



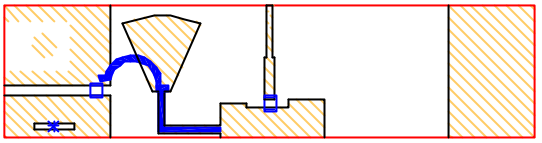
Transistor Impedance Matching

A good approach to designing matching networks is to first resonate the imaginary portion of the load impedance, then transform the resulting real impedance using low pass impedance matching sections. The first element is normally a series component or series transmission line if the real part of the load impedance is relatively constant versus frequency, or a shunt component or shunt transmission line if the real part of the load admittance is relatively constant. The optimum load impedance of high power microwave transistors is very low, often near 1 ohm. When the impedance is low and close to the real axis, it is usually impossible to make or connect low impedance shunt transmission lines. Therefore, most practical matching networks use a low impedance series transmission line as their first matching element. Remaining sections consist of alternating high and low impedance transmission lines that approximate series inductors and shunt capacitors. Sections can be optimized using a Smith chart, or design automation software.

In some cases, lumped components can be added to a distributed network to reduce size. Before using lumped matching components, they must be characterized in terms of both impedance and loss. These components are often added at low impedance points so circulating currents are high. Very low loss is required. Parasitic series inductance, and inductance of ground returns (vias) must also be low. Parasitics must be well characterized so they can be taken into account during analysis.

A typical collector-matching network for the IB3134M100 output transistor that results from this procedure is shown below.

Figure 2 – Proposed IB3134M100 Output Matching Network.



The input matching network is designed in a similar way. "Load pull" data determines optimum input impedance. In this case, a break apart circuit is tuned to minimize input return loss, and then the impedance looking back into the input matching network is measured. Some designers do a source pull characterization, but this is primarily done for linear amplifiers where source impedance may affect distortion. Input circuits of pulsed class C amplifiers are normally just optimized for match. Data can be taken frequency by frequency when output impedance is characterized. While there is some interaction between input and output networks (transistors aren't unilateral), input match is less critical and can normally be characterized for just one point at each frequency (i.e. point corresponding to best match). After optimum input impedance is determined, a matching network is synthesized as described above.

Bias Circuits

Class C bias is normally applied to bipolar transistors by connecting a low resistance RF choke between their base and emitter terminals. This biases them into cutoff. This amplifier's transistors are in the grounded base configuration, so their bases (flanges) are directly connected to ground. It is only necessary to connect their emitters to ground through a low resistance chokes. Inductance between emitter and base must be controlled, however, because it affects pulse rise and fall times. When a transistor turns on at the beginning of a pulse, changing current induces negative base-emitter bias. This holds the transistor off and slows rise time. As the transistor turns off at the end of a pulse, changing current induces positive base-emitter bias and first holds the transistor on, and then speeds fall time as current drops. Low base-emitter return inductance minimizes both effects. Total emitter to base inductance includes all inductance to the point on the emitter circuit where a shunt inductor attaches. The RF choke should be as small as necessary, and attached as close to the transistor as possible to minimize total inductance. These are primary considerations for emitter bias.

The collector supply is connected to the collector terminal through a RF choke, and then bypassed by capacitors that lower supply impedance over the video bandwidth of the signal. Video bandwidth depends on pulse characteristics. The 100 nS rise time specification for this amplifier implies video bandwidth exceeds 10 MHz. This is not a particularly difficult requirement. The collector bias circuit should include bypass capacitors that operate at low, mid and high frequencies because parasitics and losses tend to make capacitors frequency limited. Bypassing should also cover the operating frequency so the signal doesn't couple between stages on the bias line. Finally, adding a series R-C network from the collector bias line to ground often suppresses instabilities by presenting a real load impedance at frequencies outside bypass capacitor range. The R-C network, if added, is experimentally determined.

Optimization

As individual stages are designed, their circuits are constructed and evaluated. Evaluations are initially completed by constructing each stage as a break-apart circuit. This allows input and output matching networks to be characterized using a network analyzer. If analyzer plots indicate match is as expected, the stage can be assembled with active components, and then fine tuned by trimming transmission lines or other components. If an analyzer plot indicates the circuit does not present expected (designed) impedances, the circuit is examined to correct the problem; then the active stage is assembled and fine-tuned.

Combining and Cascading

Gain stages are paralleled to achieve higher output power. There are a number of methods of combining power. In general, at microwave frequencies, splitters and combiners fall into one of two categories; in-phase and quadrature combiners. The Wilkinson hybrid is a common in-phase N-Way splitter/combiner. It has the advantage that it is broadband, relatively easy to construct, and provides isolation between output ports. It is difficult, however, to add isolation resistors on planar substrates when more than 2 split ports are needed. More important, Wilkinson's don't isolate reflections from output ports to the input port. Quadrature hybrids are somewhat more complex to construct, but they isolate common reflections (i.e. have high input return loss even when split ports are terminated in mismatched loads) provided output ports are terminated in nearly the same impedance (i.e. equal in magnitude and phase). The isolation property of quadrature hybrids makes it easy to cascade quadrature combined stages because each cascaded port presents a good 50 ohm impedance to adjacent stages.

It is common to experience mismatch at the input and output ports of single ended stages. Mismatch causes mistuning of adjacent stages, and sometimes induces instability. This can be avoided by adding either an isolator or attenuation between stages to improve interstage match. Mismatch increases as bandwidth increases. It is therefore good practice to use one of the following methods when interconnecting broadband stages:

Configure each stage as quadrature combined transistors so input and output return loss is a function of the hybrid, not of the transistors.

Add isolators between stages.

Add loss between stages. It's good to target 16 dB minimum return loss for each individual stage. If a transistor and matching network have only 12 dB minimum return loss, 2 dB attenuation is needed to reach the recommended minimum.

When all stages meet target performance, they are connected as a single amplifier and fine-tuned to compensate for effects of inter-stage impedances. An alternative procedure is to lay out a complete multistage prototype amplifier and then fine tune the prototype. When laying out multistage amplifiers, it is good practice to add test ports. Test ports are formed by running 50 ohm lines close to the signal path, and in the proximity to natural break points. For example, a 50 ohm line can be run perpendicular to the midpoint of an inter-stage blocking capacitor. The capacitor can either connect the through path (i.e. normal connection) or be moved to connect to the test port. Ideally, test ports access every inter-stage point to allow single stage alignment and/or troubleshooting the amplifier.

Gain Equalization

Broadband amplifiers have higher gain at low frequencies due to characteristics of active components as well as higher loss of transmission lines at higher frequencies. Higher gain will cause overdrive of cascaded stages. This condition compounds as number of stages increases. If stages are formed using quadrature combined transistors, it is possible to design input matching circuits that reflect power to the isolated port at lower frequencies. An alternative approach is to design amplitude equalization networks that absorb power at low frequencies. Equalization networks must be designed for little or no loss at high frequencies. The latter method is suitable for cascading single ended stages because lossy sloping networks also improve match (i.e. sloping network attenuates at low frequencies). It is important to equalize stage by stage so each saturates at the anticipated operating level. If a single equalization network is cascaded with a

multistage amplifier, one or more stages will likely be under driven at some frequencies. Under-driven stages produce poor pulse shape, and their performance varies more over temperature because they have no gain compression.

Prototype Performance

To a first approximation, prototype amplifier performance should closely match summed performance of individual stages. Deviation is normally caused by:

Load Mismatch: Individual stages were characterized into a 50-ohm load. Input return loss of individual stages is often 10 dB or less (i.e. 2:1 VSWR) at some frequencies. This mismatch causes changes in gain, pulse fidelity and saturated power of adjacent stages. The effect of load mismatch can be evaluated by characterizing each stage into the minimum anticipate return loss of the succeeding stage. This is just a load pull characterization. As mentioned previously, adding an attenuator or isolator between stages minimizes inter-stage mismatch.

Coupling Around or Between Stages: Unenclosed multi-stage amplifiers tend to be stable provided their layout prevents feedback around or between stages. Little change is experienced when the sum of coupled signals is at least 15 dB below the normal input level. For example, a 25 dB gain amplifier will be stable and show little change in response if stray couplings to the input of each stage are below –15dBc compared to the signal input.

When an amplifier is enclosed, cavity effects can alter response. Enclosures often resonate at one or more frequencies. At resonance, response changes and instability may occur. There are several methods of eliminating cavity effects. One is to partition an amplifier. Signals are fed through small cutouts between stages. Cutouts act as below cutoff waveguide and effectively isolate partitioned stages except for the intended, transmission line coupled signal.

When it's not possible to add solid partitions, adding posts often helps suppress modes. Posts are low inductance paths that effectively short across a cavity. Posts should run across the short dimension of an enclosure. Placement and number are usually experimentally determined.

Power Supply Coupled Signal: Bias lines in multi-stage amplifiers must be adequately bypassed over the operating frequency range to prevent RF from coupling to other stages. A common method is to bypass bias lines using series resonant, low ESR capacitors at every DC feed point. Series resonance can be estimated using a capacitor's model, but should be verified by measurement since ground inductance (e.g. via inductance) lowers series resonance.

Summary

This paper described solid state radar amplifiers and outlined a procedure for their design. Design starts with the development of a block diagram that breaks overall performance into component and circuit requirements. The paper focuses on design of solid state circuits, and emphasizes the need to characterize all components to understand and predict their RF characteristics. It briefly mentions problems associated cascading and paralleling and stages. The paper is illustrated by a hypothetical SBand, multi-stage RF power amplifier.

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