Characteristics of Microwave Power GaN HEMTs on 4-Inch Si Wafers

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Abstract — **We present the design and development of AlGaN/GaN high electron mobility transistors (HEMTs) fabricated on a 4-inch Si wafer. The GaN HEMT devices demonstrate a maximum drain current of 900 mA/mm, a peak g_m of 300 mS/mm, and a microwave output power density of 1.5 W/mm. To the best of our knowledge, these are the best results reported on GaN HEMTs on 4-inch Si wafers.**

I. INTRODUCTION

Recent progress in the growth of wide bandgap (WBG) semiconductor materials such as SiC and GaN demonstrates the potential of this technology for high power microwave applications. Most GaN-based HEMT devices to date have been produced on Sapphire or SiC substrates due to the limited availability of bulk GaN substrates. While GaN HEMTs have demonstrated remarkable performance on Sapphire (4.2 W/mm at 4 GHz [1]) and SiC (6.9 W/mm at 10 GHz) [2], the commercial viability of devices grown on these substrates is hampered by cost and high-volume manufacturing issues. However, the use of a mature technology like silicon as the substrate material offers a clear commercialization pathway in terms of large-scale wafer fabrication and low-cost manufacturing.

In this paper, we report the development and characterization of AlGaN/GaN HEMTs on Si. The GaN HEMT devices demonstrate a maximum drain current of 900 mA/mm, a flat g_m of 300 mS/mm and a microwave power performance of 1.5 W/mm at 2 GHz. We provide detailed small signal, large signal and transient characterization of AlGaN/GaN HEMTs on large scale Si wafers. The electrical performance of these devices exemplifies the viability of silicon as a low-cost platform for AlGaN/GaN HEMTs.

II. MATERIAL GROWTH AND DEVICE FABRICATION

The key to successful fabrication of GaN heterostructures on silicon lies in the accommodation of the large thermal and lattice mismatch between Si and GaN. GaN layers are grown directly on silicon wafers by an MOCVD technique using a transition layer scheme, which addresses these mismatches in the material system. The HFET structure deposited on the GaN layer consists of an undoped AlGaN spacer layer, an AlGaN donor layer, an undoped AlGaN followed by GaN cap layers. Figure 1 provides a schematic view of a cross-section of the device.

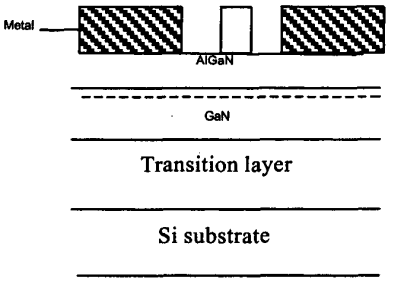

Figure 1. A cross section of a AlGaN/GaN HEMT on Si

The devices were fabricated using contact lithography techniques along with a typical GaN liftoff based process. Source and drain ohmic contacts were fabricated by evaporating Ti/Al/Ni/Au followed by annealing for 30 sec. at 900°C. Dry etching of mesa structures in a RIE system employing a chlorine-based chemistry was used for device isolation. Ni/Au was used for the schottky gate metallization. Finally, the active

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devices were passivated with silicon nitride after the gate contacts were in place.

Additional details on the fabrication procedure are reported elsewhere [3]. The fabricated devices were then characterized under DC, small signal and large signal conditions.

III. DC AND TRANSIENT ANALYSIS

Typical static characteristics of the AlGaN/GaN HEMT on Si for 200 μm devices are shown in Figure 2. The threshold voltage for the devices was –3 V and the breakdown voltage at pinch-off was found to be 22V. The devices exhibited a saturation current of 662mA/mm and a maximum drain current of 887mA/mm. The transfer characteristics of the GaN HEMT are shown in Figure 3. The peak extrinsic trans-conductance was found to be 288ms/mm at a gate-source voltage of –1.5V.

Although the static characteristics are comparable to previously reported results of AlGaN/GaN devices on sapphire and SiC, the microwave characteristics of the device are affected by parasitic loading through the conductive substrate in addition to the well-known DC-RF dispersion arising from trapping effects. In order to understand the extent of the influence of the respective effects, the transient and small signal characteristics of the device were investigated.

In III-V technologies gate lag measurements are more sensitive to surface trapping effects and drain lag effects are more sensitive to buffer-layer trapping effects [4]. Surface trapping leads to a 'lag' or a slower drain current response to a polarity reversing signal at the gate restricting microwave output power. Buffer trapping leads to an increase in knee voltage and a reduction in maximum current thus restricting output power. Figure 4 shows the gate lag measurements on a 200 μm device. The gate source voltage was pulsed from the threshold voltage to 0 V while the drain source voltage was held constant. It must be noted that the pulse width is short relative to the time constant of the gate lag, which is why one cannot observe the minimal 'lag' for the structure [5]. The drain current is normalized to the static current value. For a short pulse width any lag in the current response would be seen as a drop in the peak current value from 1. Thus, one observes a near-ideal gate lag response in the passivated devices indicating minimal surface trapping [4].

Drain lag measurements were conducted on the same devices. The drain step amplitudes were 8, 10 and 12 V for a gate-source voltage of 0 V. Frequency dispersion of the output conductance corresponds to the small signal limit of the drain lag phenomena. Ideally, in the absence of parasitic loading effects, the drain current must not increase with decrease in pulse width beyond a certain point (typically microseconds) as the trapped charge cannot respond to a rapidly changing voltage.

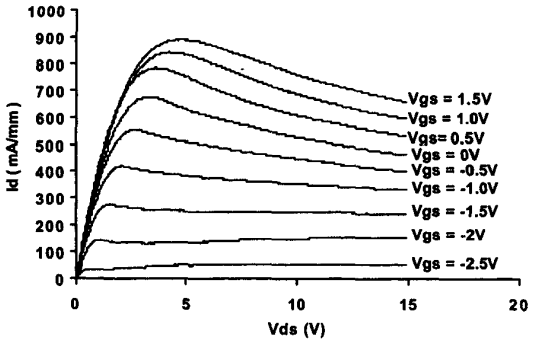

Figure 2. Measured I-V characteristics of the AlGaN/GaN HEMT on Si substrate for a gate width of 0.2 mm.

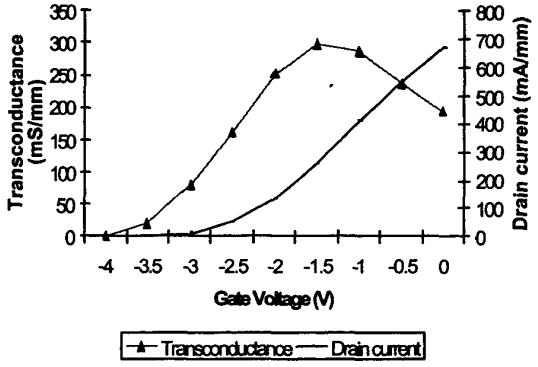

Figure 3. Transfer characteristics of the AlGaN/GaN HEMT at a drain source voltage of 15V. The peak extrinsic trans-conductance was found to be 300ms/mm.

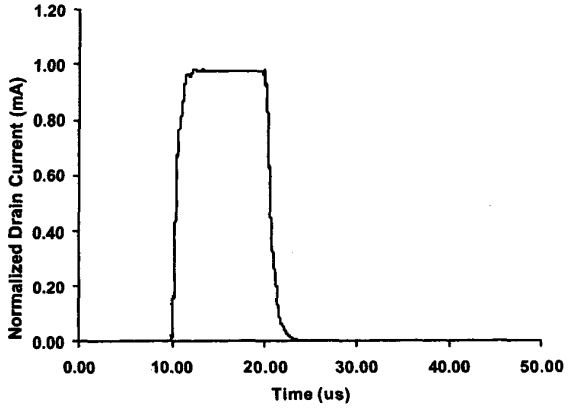

Figure 4. Gate lag response for the AlGaN/GaN HEMT. The response was found to be near ideal after passivation.

However, one noticed an increase in the drain current as the pulse width is reduced indicating a change in the output conductance. This can only be attributed to the reflection of the substrate's conductivity by the parasitic p-i-n diodes (p-Si/GaN insulator/metal pads) at the off-mesa metal pads as suggested in [6].

IV. LARGE-SIGNAL CHARACTERIZATION

On-wafer load-pull measurements were conducted to determine the continuous waveform output power. Focus Microwave computer controlled microwave tuners were used in this measurement. The device was biased in Class A operation with a drain source voltage of 15 V and a gate source voltage of –1.5 V. A power added efficiency of 26% and a power density of 1.5 W/mm at 2 GHz was observed as shown in Figure 5.

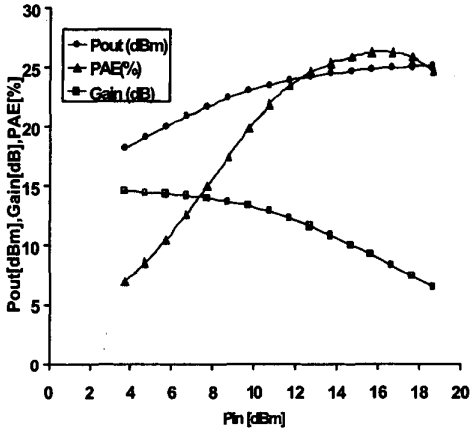

Figure 5. Class A Load-pull measurements on a 200 μm HEMT. The power density for the measured devices is 1.5 W/mm at 2 GHz and the PAE is 26%.

For a FET biased in class A, the output power can be estimated from the static characteristics as in [1]:

$$P_{out} = I_m \frac{V_b - V_{Knee}}{8} \quad (1)$$

The calculated theoretical output power was found to be roughly 2.5 W/mm. However the maximum output power obtained from the devices was 1.5W/mm. As previously discussed, transient analysis indicates that DC-RF dispersion arising from trapping effects in the surface and the bulk of the semiconductor are not enough to explain the reduction in power density. Previous work indicates that the conductivity of the silicon substrate causes capacitive charge coupling and parasitic loading of the device [6]. To gain an insight into the strength of this loading, an equivalent circuit model of the device was developed.

V. SMALL SIGNAL ANALYSIS

S-parameter measurements under Hot-FET, pinched-off Cold-FET and forward bias cold-FET conditions were taken for the 200 μm device with the help of an 8510C ANA and on-wafer coplanar probes. With a conductive substrate like silicon, the p-Si/GaN/metal structure at the metal pads effectively acts as p-i-n diodes in series with resistors reflecting the substrate conductivity and loading the device. These are modeled as R-C networks with the number of R-C chains in the model indicating the strength of the parasitic loading effect. The topology of the equivalent circuit model is shown in Figure 6.

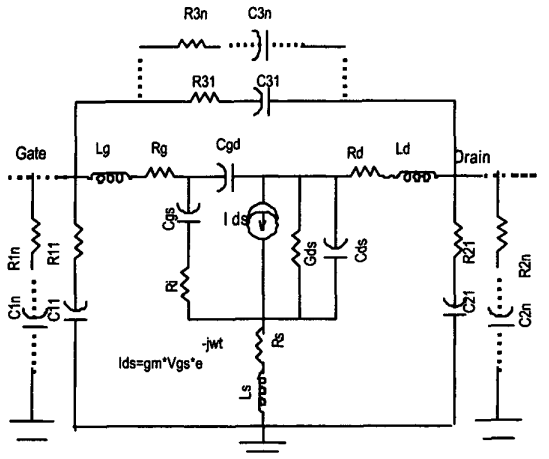

Figure 6. Equivalent circuit model topology for the AlGaN/GaN HEMTs on silicon substrate.

Under forward bias conditions and low frequencies, the RC network was found to have minimum effect on the Z parameters. Conventional Cold-FET techniques were used to extract the parasitic resistors and inductors. Pinched-off cold FET measurements were then taken. As the parasitics in the RC network are assumed to be independent of bias, determining their value by optimization under Cold-FET conditions is much simpler as the number of unknowns is reduced. Optimization was done using a commercial CAD tool. Once a good fit to the measured S-parameters under cold FET conditions was obtained, all the extrinsic parasitic elements are fixed and are then de-embedded from the Hot-FET measurements from which the intrinsic FET parameters are determined. The parameters of the equivalent circuit model of the FET are summarized in Tables. 1-3. The agreement between

measured and modeled S-parameters up to 18 GHz is shown in Figure 7.

TABLE 1
EXTRACTED INTRINSIC ELEMENT VALUES FOR THE AlGaN/GaN HEMT

gm (ms)	Tau (psec)	R_{ds} (Ω)	C_{gs} (pF)	C_{ds} (fF)	C_{gd} (fF)	Ri (Ω)
53.13	2.89	984	0.6	80	35	5.04

TABLE 2
EXTRINSIC ELEMENT VALUES

L_g (pH)	L_d (pH)	L_s (pH)	R_g (Ω)	R_d (Ω)	R_s (Ω)
71	103	12	2.35	2.89	0.966

TABLE 3.
R-C ELEMENTS

C_{11} (fF)	C_{21} (fF)	C_{31} (fF)	R_{11} (Ω)	R_{21} (Ω)	R_{31} (Ω)
230	120	10	208.82	155.39	53.89

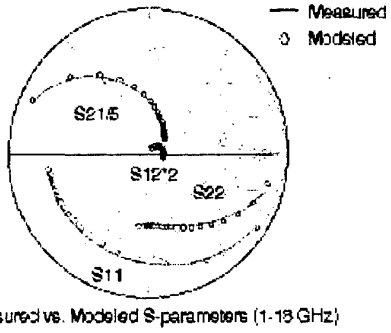

Figure 7. Agreement between measured and modeled S-parameters up to 18 GHz

As the strength of the parasitic loading is expected to scale with device size, the elimination of these effects by increasing the substrate resistivity is crucial to subsequent improvements in microwave performance. It is anticipated that further improvements in power density will be made possible by taking advantage of silicon wafer bonding technology and incorporating high resistivity substrates.

VI. CONCLUSION

In this paper, the design, development, and characterization of GaN HEMTs on 4 inch Si wafers has been presented. The devices exhibited a saturated drain current of 600mA/mm, a maximum drain current of 900mA/mm and a transconductance of 300mS/mm. the electrical performance of the AlGaN/GaN HEMTs on Si reveals the viability of these devices in microwave power applications. However, transient and small signal analysis indicated that the microwave output power was primarily limited by parasitic loading from the substrate that must be eliminated in order to achieve better performance.

ACKNOWLEDGEMENT

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