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Application Note 55

On Wafer Load Pull of Sub-Ohmic Power Chips

Summary

A measurement set-up is presented, which allows accurate load pull testing of wafer chips with internal impedances of less than 1Ω*. The technique uses a combination of passive tuners and an active reflection factor-enhancing module. The test unit requires only standard off-the-shelf components and a power amplifier in the active section, which provides no more power than the test device itself. The proposed set-up can be used up to and beyond frequencies of 40GHz.

Introduction

Load pull testing of high power chips on wafer is a measurement challenge for which a satisfactory and affordable solution has not yet been presented. Testing transistor chips on wafer with internal impedance of less than 1Ω is not possible using exclusively passive tuners. Insertion loss of micro-probes and, even very low loss connections to the tuners limit the minimum attainable impedance to more than 2Ω at frequencies around 2GHz and 5Ω or higher above 20GHz. Active load pull set-ups, on the other hand, though offering, in principle, a solution are cumbersome, require costly external power amplifiers and contain systemic measurement error sources, which have been discussed at length in reference [1].

Figure 1: On wafer set-up using passive tuners and Γ_{Load} enhancing active power section

**Patent pending*

Principle of Operation

The On Wafer Load Pull System of Sub-Ohmic Power Chips is shown in Fig.1. It consists of three sections, from the DUT to the load as follows:

- the prematching tuner,
- the active section (box), and
- the load tuner.

The active section includes a driver amplifier, band-pass filter and isolators at the wanted frequency (figure 2). The performance of the system is determined by those components. The setup allows, due to signal amplification, increasing the reflection factor, seen by a DUT, to higher level than with passive tuners alone. The RF signal injected from the RF generator into the DUT, after amplified by the DUT, is reflected by the load tuner (depending on the load tuner's VSWR setting), and then, after being reflected by the load tuner, it is amplified by the driver amplifier and injected back into the DUT. The result is the possibility to generate reflection factors $\Gamma>1$at DUT ref. plane. The high reflection factor, which means in fact a "perfect" system from the reflection point of view, can be achieved even if there is considerable loss between the DUT and the set-up (i.e. long cable, probe loss etc.).

Previous configurations using active modules [2] did not use a prematching tuner section and the mismatch between the (low) DUT output impedance and the active module's input impedance (50Ω) required very high power amplifiers inside the active section, in order to be able to inject linear power into the output port of the DUT. As shown in table I the linear power required from the load amplifier is typically 10 to 13dB higher than the maximum power of the DUT.

The proposed On Wafer Load Pull System of Sub-Ohmic Power Chips uses a prematching section between the DUT and the active section. The prematching section raises the output impedance of the DUT to a level that matches better the 50Ω internal impedance of the circulator at the input of the active section. By doing that, the required power from the driver amplifier is significantly reduced (depending on the VSWR on the prematching tuner used, see table I), thus allowing the use of affordable driver amplifiers in the load with less gain and reducing the risk of spurious oscillations.

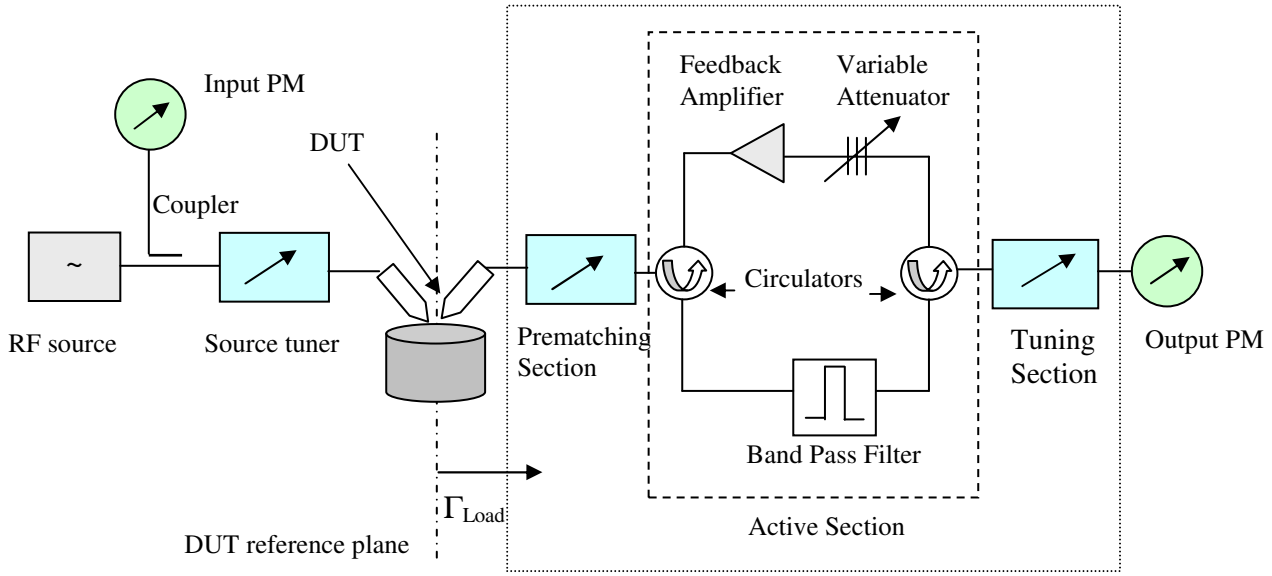

Figure 2: Principle of operation of the On Wafer Test System (as shown in figure 1)

Theoretical Analysis and Limitations

The proposed set-up includes an amplifier network in the feedback loop and can therefore create a negative impedance (i.e. Γ>1) seen from the DUT output port.
The new aspect of this set-up is the effect of the pre-matching section on the calibration points of the tuning section, seen by the DUT. We therefore analyzed the basic circuit using real measured data of a tuner, an active section and a test fixture and used the VSWR setting of the prematching section as the independent parameter.
Our analysis is based on the following block diagram:

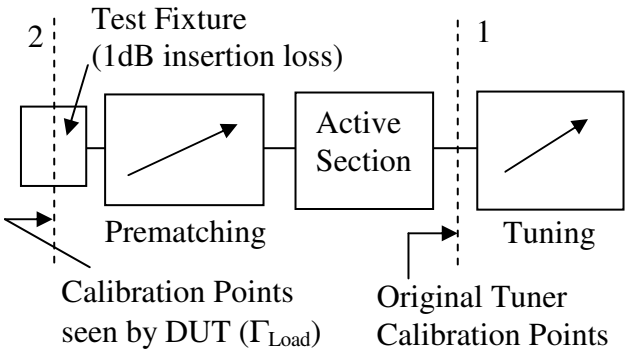

Figure 3: Configuration used for set-up analysis.

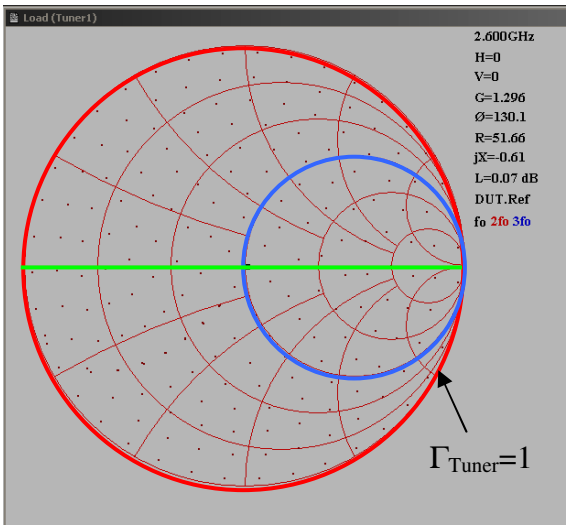

Figure 4: Tuner Calibration points seen at Tuner Reference plane (1)

The following pictures demonstrate the effect of the active section and increasing prematching on the overall calibration points, seen by the DUT (reference plane (2)).

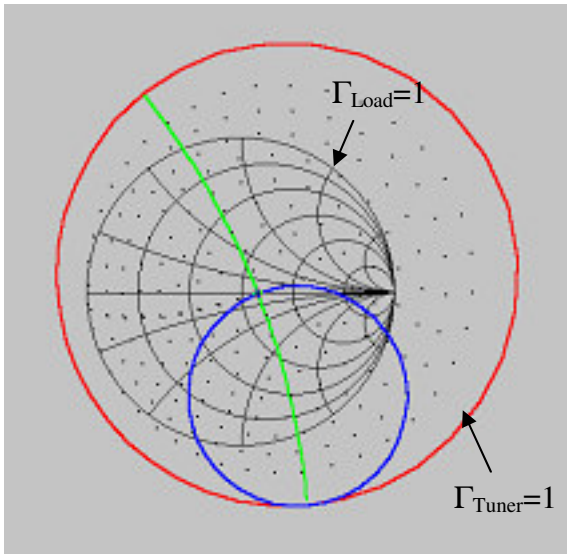

Fig 5: Tuner Calibration seen by DUT (reference plane (2)), without Prematching, VSWR=1:1 (Prematching tuner initialized)

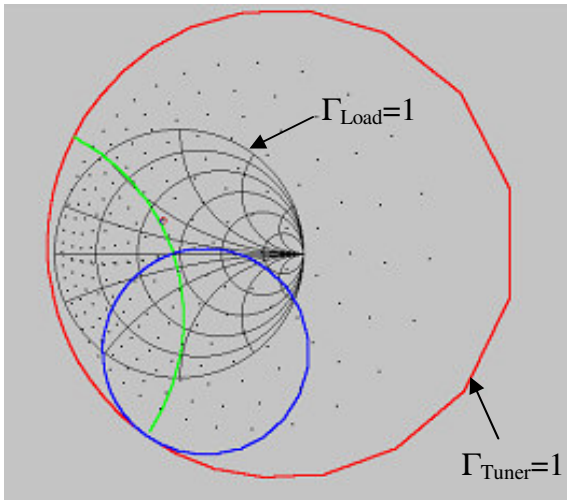

Fig 6: Tuner Calibration seen by DUT at Prematching VSWR=2:1

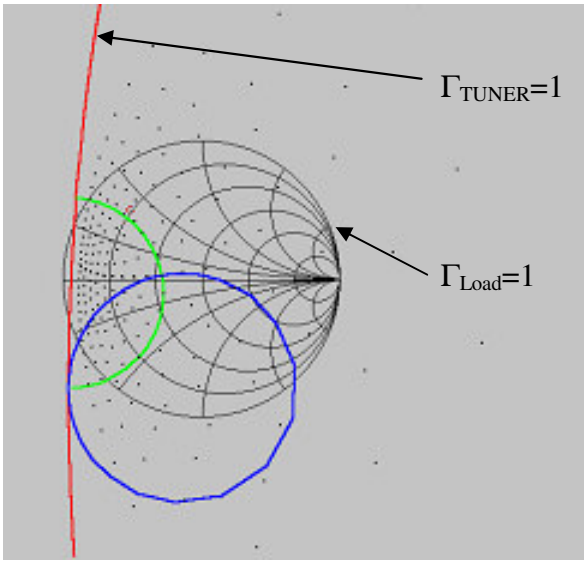

Fig 7: Tuner Calibration seen by DUT at Prematching VSWR=6:1

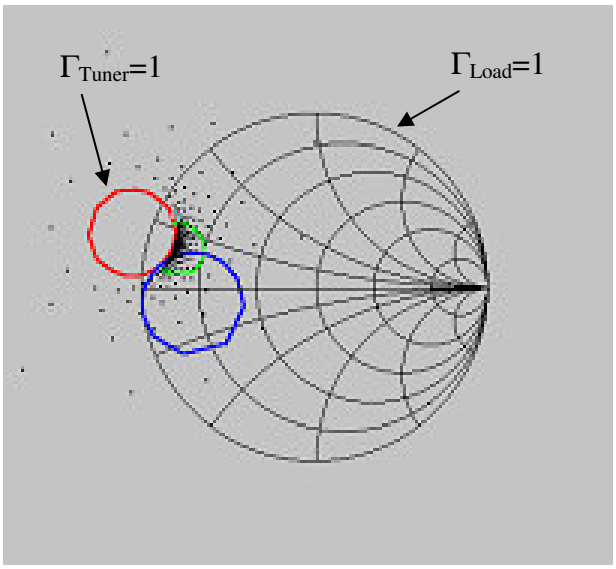

Fig 9: Tuner Calibration seen by DUT at Prematching VSWR=20:1

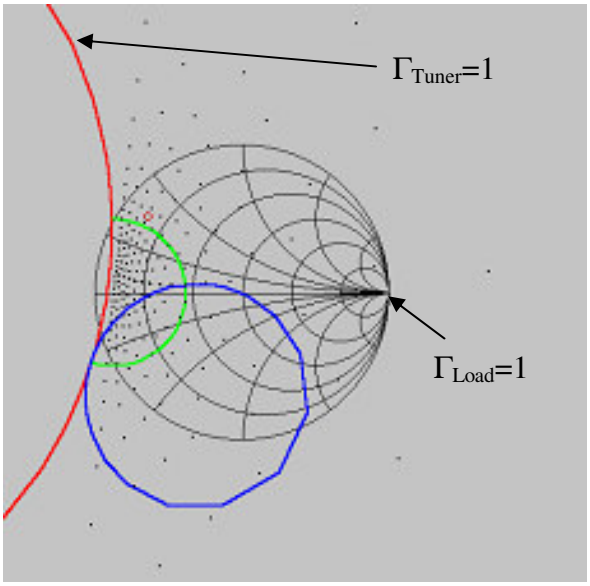

Fig 8: Tuner Calibration seen by DUT at Prematching VSWR=10:1

Figures 5-9 demonstrate the use and the limitations of this type of set-up in this practical case.
Prematching in this case when combined with the active section does behave differently than in the passive only case (see Focus Microwaves PN 52 on Prematching Tuners). Figures 6 and 7 in combination with table I show that, if both the maximum tuning range and the best power transfer efficiency are considered, the best VSWR of the prematching section is around 7:1. At lower VSWR the power required from the active section amplifier is too high (but tuning range is better), and at higher VSWR the tuning range is limited by the inversion of the generalized Smith Chart (but power transfer is better).

System Calibration and Verification

The following section outlines the procedure used to calibrate and verify the performance, linearity, accuracy and power requirements of the proposed set-up. The purpose of the verification set-up is to use a known DUT and means of measuring the power generated by the active section, in order to be able to judge about the suitability of the set-up for measuring low impedance power chips on wafer.

Set-up for Experimental Verification

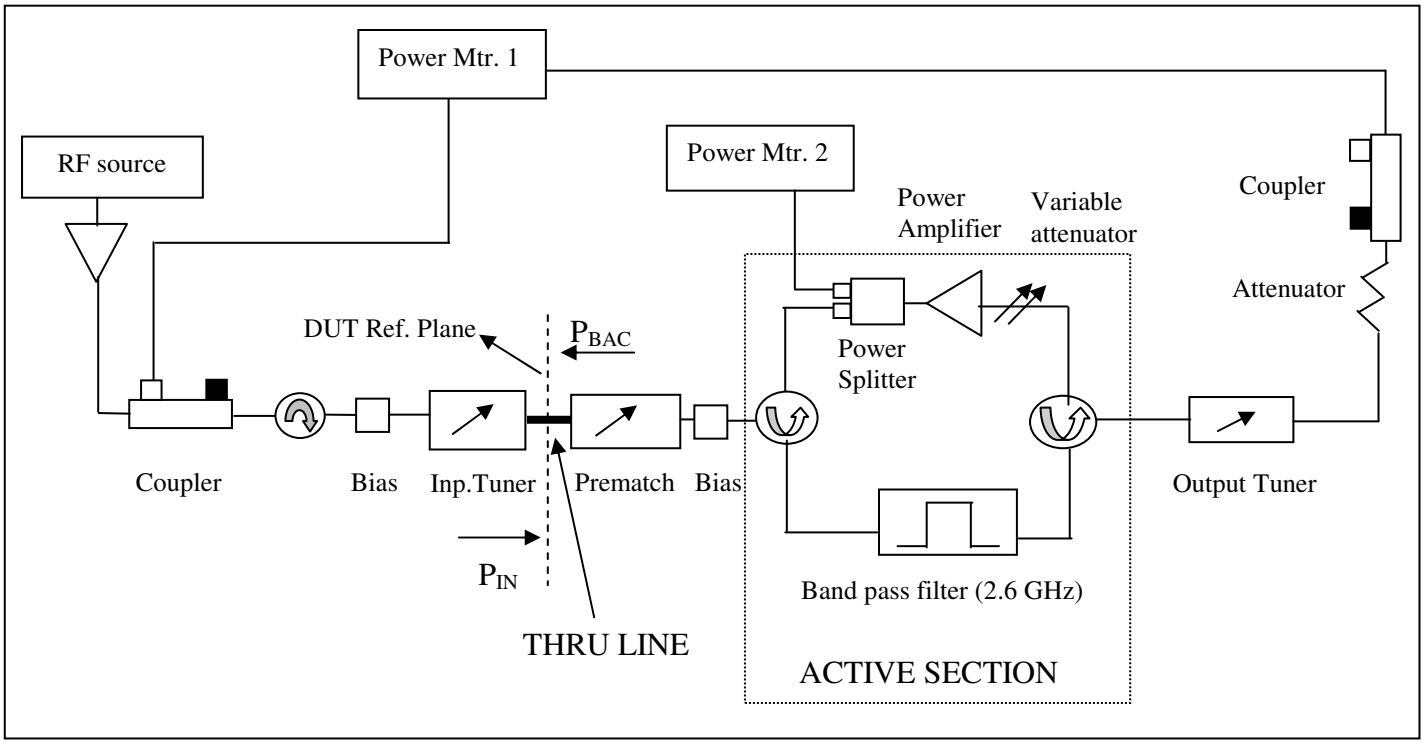

Figure 10: Experimental setup for measurement, with all the components needed; a THRU line is used as a DUT

The input part of the experimental setup shown in Fig.10 (input of the DUT) consists of coupler, isolator, DC bias tee and tuner. The output part of the setup has prematching tuner, DC bias tee, active section, manual tuner, output tuner, attenuator and coupler. External equipment is standard, like for any other load-pull measurement system (RF generator, power meter, power supply for bias, etc.). The active section determines the frequency of the setup by its internal components (filters, circulators).

As a known DUT we use a THRU line and we measure the "back" power using a power splitter connected to the output of the load amplifier (figure 10). The input tuner is used to generate a low impedance in order to simulate the output impedance of a power chip. We normally set this impedance to 1Ω. Under these conditions we can perform two verifications simultaneously:

a) We can measure the power required from

the power amplifier in the active section in order to match the 'DUT' (1Ω) impedance and

b) we can perform the 'back-to-back' test of the setup, at various source impedances (other than 1Ω).

Since $\Gamma_{Load} = P_{BACK}/P_{IN}$, it is obvious that a THRU line DUT is the appropriate test device to determine the power requirement of the amplifier and, by doing the same test at increasing source power, we can determine the limits of its linearity; this would be the case, when the automatic 'peak search' routine of the Focus load pull software starts delivering different values for the same source impedance, with increasing source power. It has to be noticed that all peak search and other tuning operations are carried out using the output tuner and not the prematch tuner. The prematch tuner is set to a certain SWR value and considered a test parameter

Power Requirements

Using a prematching section effectively reduces the power requirement of the active section amplifier by up to 12dB (at prematching VSWR=10:1).

VSWR of Prematching Sections	Input power at the DUT Output [dBm]	Power of Active Section Amplifier $P_{AM\_OUT\ [dBm]}$
1:1 (no prematching)	26.50	36.10
2.5:1	26.60	33.35
5:1	26.60	29.92
7:1	26.60	28.44
10:1 (full prematching)	26.60	24.60

Table I: Power distribution depending on the VSWR used on prematching tuner

Table I shows that, for sufficient VSWR of the prematching section, the power required from the amplifier, in order to create a reflection factor of 0.961 (Z=1Ω), may be reduced to less than the output power of the DUT. Whereas at VSWR=1:1 (no prematching section) the required linear power is roughly 10dB higher than the DUT power, at VSWR=10:1 the power required is almost 2dB less than the maximum DUT output power, and this despite the insertion loss of the tuner in the prematching section. We suggest to use VSWR=7:1 for best performance of the system, in view of the power transfer and tuning range (figure 7).

The following two saturation plots show the effect of the VSWR of the prematching section on the linearity of the system. The curve in figure 11 is measured with the prematching tuner initialised (VSWR=1:1) and in figure 12 with VSWR=7:1. It can be seen that the amplifier of the active section saturates at ~10dB higher input power (=DUT output power), all for the same load reflection factor of 0.961 (corresponding to Z_{DUT}=1Ω).

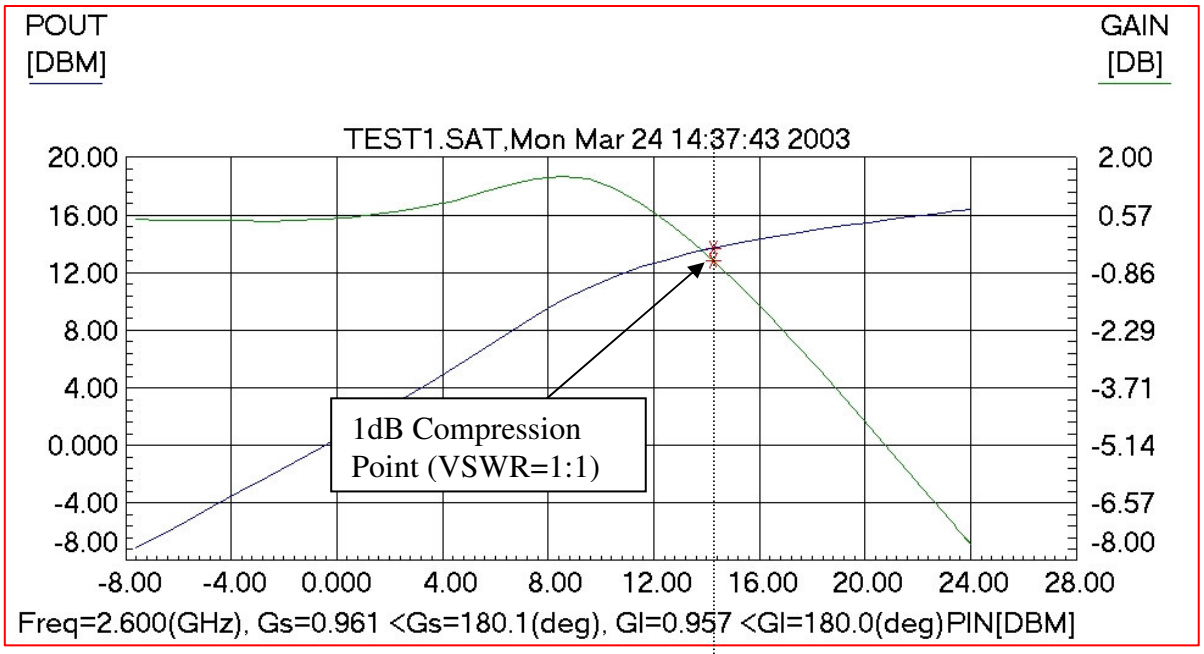

Figure 11: Saturation curves done on THRU at no prematching (VSWR=1:1)

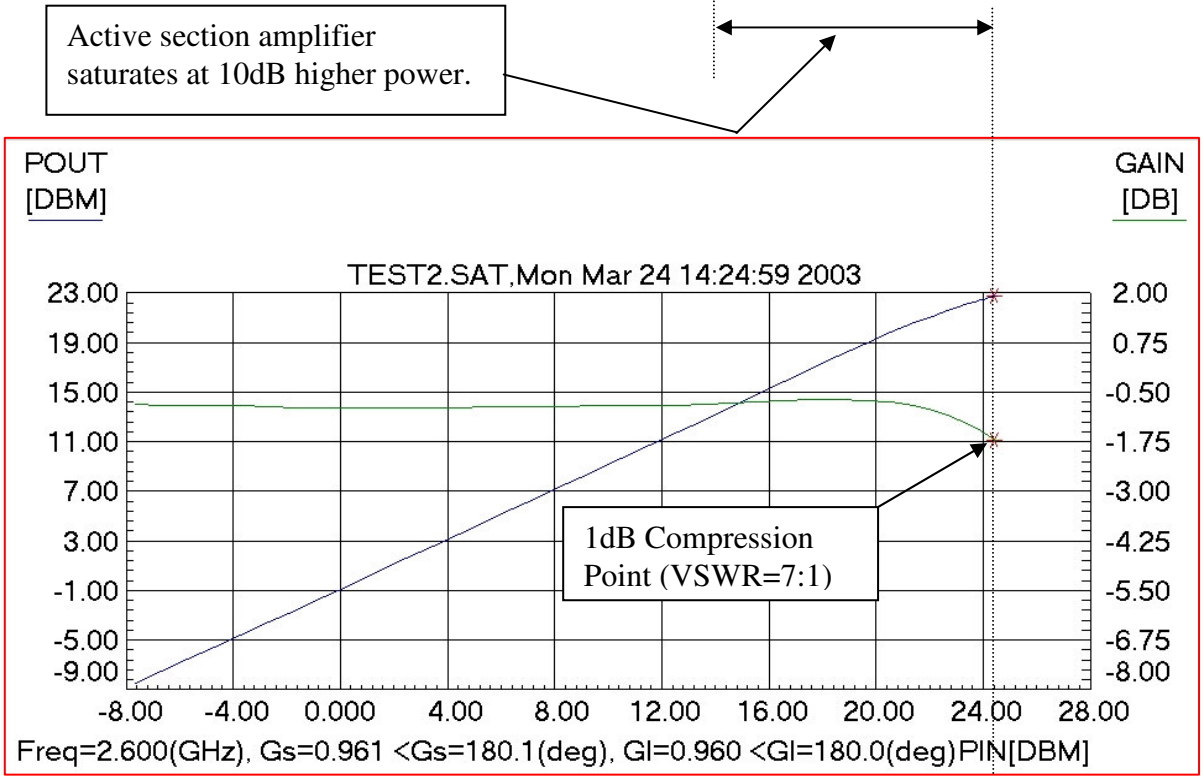

Figure 12: Saturation curves done on THRU for prematching section at VSWR=7:1

Calibration and Verification

The proposed set-up can be calibrated using any vector network analyser. The calibration can be carried through either item-by-item or "in-situ".

Figure 13 demonstrates the procedure used to calibrate the set-up "in-situ".

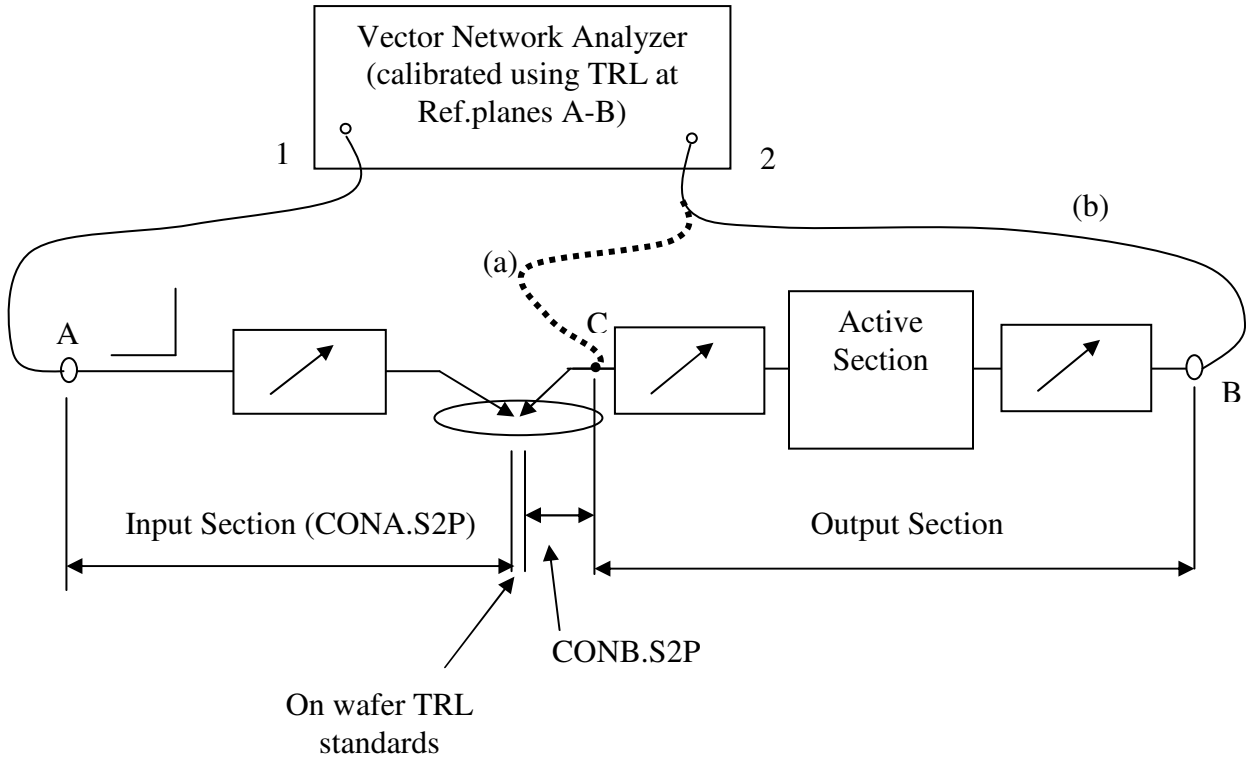

Figure 13: In-situ calibration of on-wafer set-up.

Since the active section includes nonreciprocal components (amplifier, circulators) straight TRL measurement does not apply for the Output Section of the setup. This means that the Input Section cannot be calibrated "through" the output section. In order to overcome this problem the calibration has to be done in four steps

1. Calibrate the VNA using TRL on the coaxial reference plane A-B.
2. Connect VNA cable of port 2 to point C, at the output of the test fixture (condition (a)) and run the Focus TRL on-wafer calibration (delivers CONA.S2P and CONB.S2P).
3. Calibrate the input tuner in-situ using CONB for de-embedding.
4. Connect VNA cable port 2 back to point B and cable port 1 to point C looking into the load and calibrate the output section as a prematching tuner.

This procedure requires a minimum of dis- and re-connections and therefore provides the best possible accuracy.

Verification of System Accuracy

Once the whole set-up is calibrated, the verification is done on THRU for matching conditions of one tuner by the other, including the active section. The expected gain is 0 dB. The starting point is 50Ω for both input and output side of the DUT reference plane. After that, Γ is gradually increased on the input side and output side is tuned to the conjugate complex value. As long as the gain is close to 0dB we consider that the system is accurately calibrated. For every position of the input tuner, the peak search routine can be performed on the output side, looking for the optimum position (e.g. max gain, which is 0dB for the THRU). Gain values in the low tenth of a dB range are acceptable when reached at impedance values below 2Ω. The cause for such deviations is complex and has to do not necessarily with the tuner calibration alone, but all other imperfections and disconnections of the set-up (including the output impedance of the source driver amplifier, which is difficult to measure accurately at high power).

System Linearity and Test Results

The measurements of the device in the test set-up can only be performed for power ranges that assure that the driver amplifier, which is used as a part of an active module, is in the linear area. Linearity must be verified in terms of insertion gain and of phase. The amplifier is considered 'linear' as long as its gain and transmission phase do not change noticeably. Figures 14 and 15 show the saturation curves of the driver amplifier used for this experiment. They show a linearity limit of approximately 30-31dBm (1-1.2Watts). At an output power of 29.7dBm the transmission phase is constant within 0.1° (dotted line in figs. 14 and 15). As discussed on page 4 the optimum VSWR of the prematching section is a compromise between required output power of the amplifier and the Smith Chart coverage at the DUT ref. Plane. At VSWR values >8:1 sections of the Smith Chart remain uncovered. The optimum VSWR values are between 5:1 and 7:1.

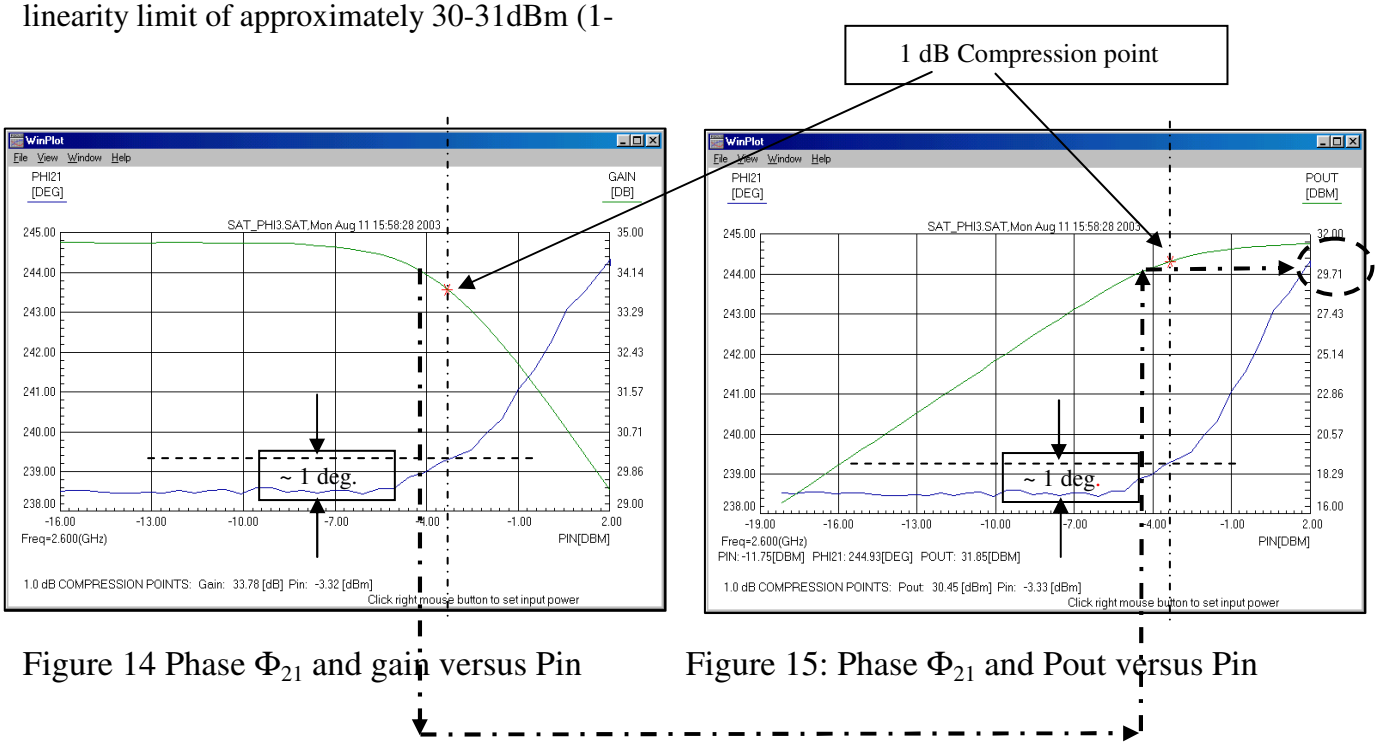

Figure 14 Phase Φ_{21} and gain versus Pin

Figure 15: Phase Φ_{21} and Pout versus Pin

The results shown below are produced for two FET devices, EPA*120B*-100F (29dBm nominal output power) and EPA*240B*-100F (32.5 dBm nominal output power). Each device has been tested both in the linear and saturated power range.

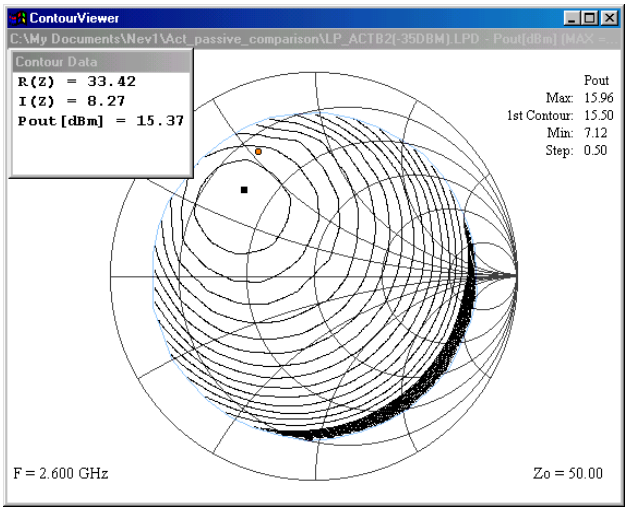

Figure 16: EPA*120B*-100F – linear range

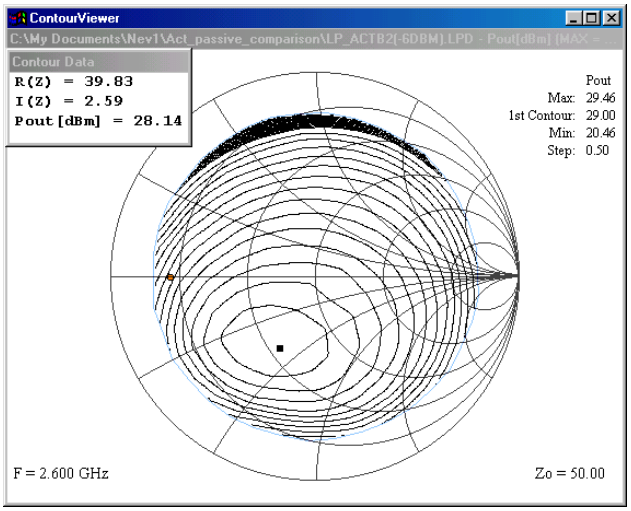

Figure 17: EPA*120B*-100F – saturated

Figures 16 and 17 show the load pull result of the FET type device in its linear and non-linear range of operation. These devices do not have a very low impedance, so the full capacity of the test system in terms of very high Γ did not need to be employed. The devices used for tests had typically about 0.8W output power (EPA*120B*-100F), and 1.8W respectively (EPA*240B*-100F). This, of course, depends on the frequency used. The power amplifier in the active section (figure 2), which is an integral part of the system, was driven only up to 1.6W. This proves the theory that for using this system, this amplifier does not need to provide more power than the DUT. Fig.18 below shows the full extent of tuning range that can be achieved using the test system. It could test transistors with internal output impedances as low as 0.17Ω.

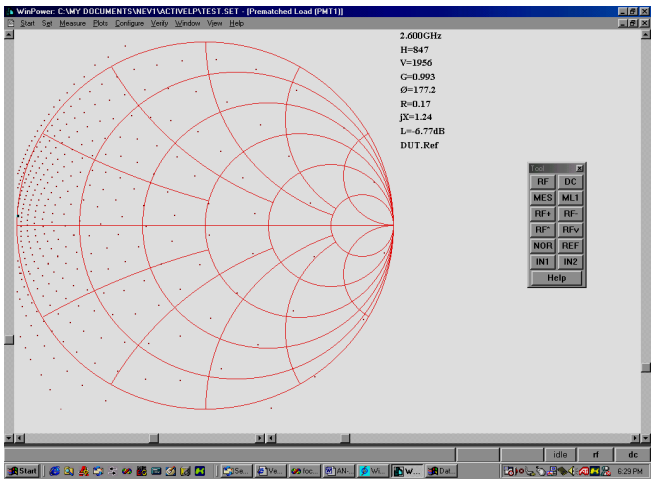

Figure 18: Reflection factor Γ can reach 1 (total reflection), enabling characterization of very low impedance devices

All results of the active system presented here, have been verified using a passive system, under the same conditions (same frequency, input power, bias, source impedance). Fig.19 shows load pull contours produced using the active system for the EPA*240B*-100F in 1dB compression. Fig.20 shows load pull contours for the same device, under the same conditions, but taken using the passive system (i.e. tuning only with the tuner of the prematching section). It is clear that the results are virtually identical.

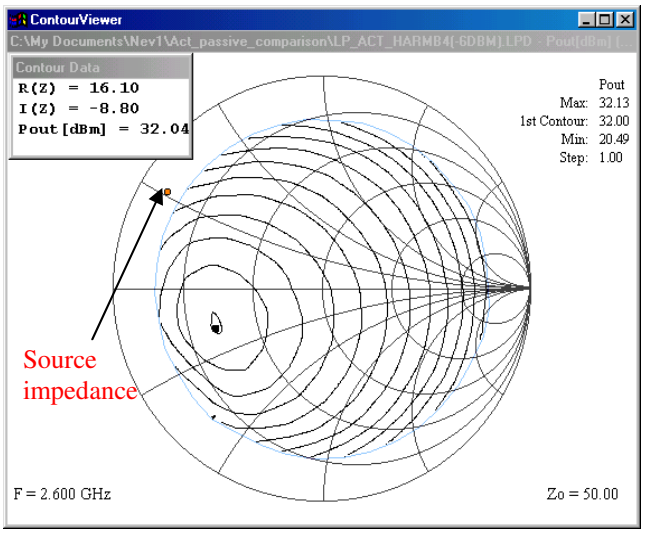

Figure 19: EPA*240B*-100F, active system

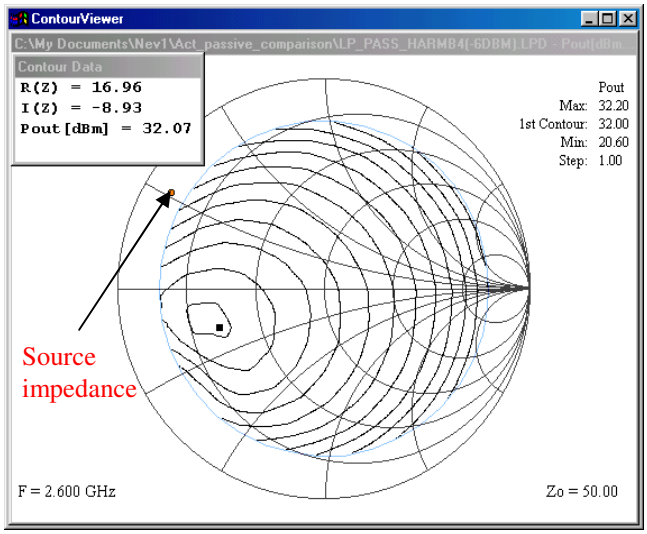

Figure 20: EPA*240B*-100F, passive system (with harmonic tuners)

An interesting phenomenon has been noticed, while performing the load pull measurements using the active and the passive system in the highly saturated area of the devices (fig. 21): Here, the effect of tuning the second and third harmonic is important. In the active system the harmonic impedances are fixed, due to the pass-band filter, which stops harmonic signal components from reaching the load tuner and bouncing back. In the simple passive system version however, when only the prematching tuner is used (which is a wideband device, with 'uncontrollable' reflections at the harmonic frequencies), the corresponding contours appear distorted (figure 22). In order to correct this measurement error we used one of Focus' harmonic rejection tuners in order to stabilize the harmonic impedances (figures 21 and 22).

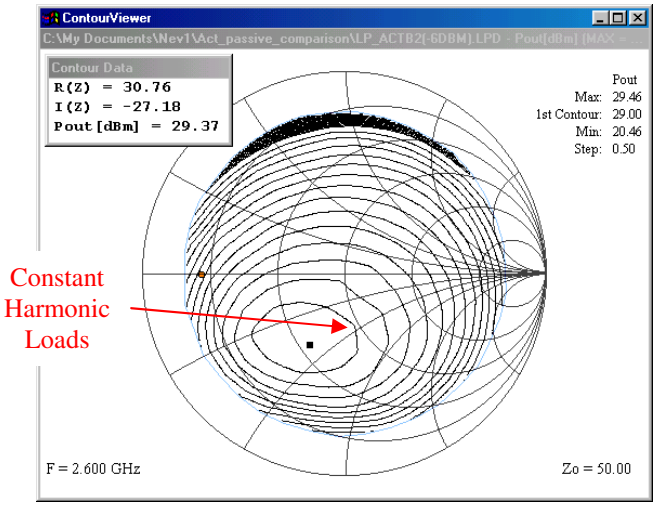

Figure 21: EPA*120B*-100F, active system

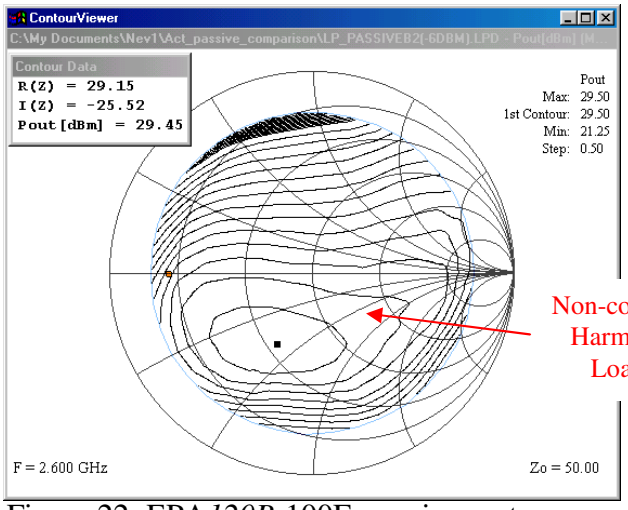

Figure 22: EPA*120B*-100F, passive system (without harmonic tuners)

Conclusions

A test set-up is presented, which allows for on-wafer load pull of sub-Ohmic devices.
The set-up uses an active section, which allows filtering and amplifying the signal, returned by a load tuner. This way the set-up is capable of generating reflection factors >1, thus allowing for compensation of cable and probe losses, which, at high frequencies, become critical.
The set-up employs also a fully calibrated pre-matching stage between the DUT and the active section, thus reducing the requirement for high linear power of the amplifier, embedded in the active section, to a level equal to or less than the output power of the DUT itself.

Literature

[1] Active Load Pull Systems: Strengths-Weaknesses-Alternatives
http://www.focus-microwaves.com/News/NewsLinks/alp-str-weak.html

[2] "Active Modules for Harmonic Load Pull Measurements", Product Note 42, April 1997, Focus Microwaves.

[3] "Prematching tuners for very high VSWR and power load pull measurements", Product Note 52, March 1999, Focus Microwaves.