1603 St.Regis
D.D.O., Quebec H9B 3H7, Canada
Tel 514-684-4554 Fax 514-684-8581
E-mail: info@ focus-microwaves.com
Website: http://www.focus-microwaves.com

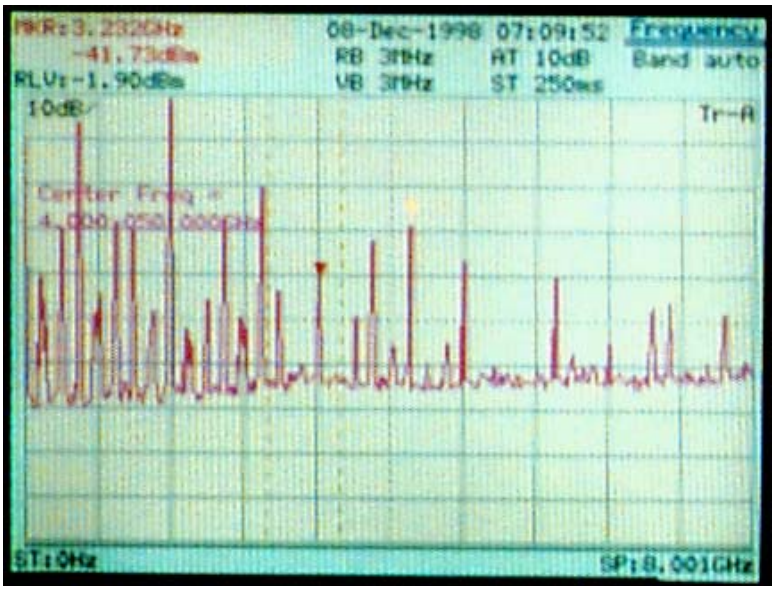
Application Note 54

Spurious Oscillations during Load Pull

Introduction

Load Pull consists of manipulating the source and load impedances of transistors in order to optimize their RF performance. Most of the Smith Chart area is covered automatically using tuners, and a number of RF and DC parameters are measured for generating ISO contours and other plots. Since most tuners used are very wideband devices and test setups not ideal, spurious oscillations during the test are a common, annoying and dangerous, phenomenon; spurious oscillations either falsify the results or cause the transistors to breakdown and burn out. It is important to realize, from the beginning, that oscillations typically occur at frequencies other than the test frequency, in general somewhere in the range of a few to a few hundred MHz, where the gain of the transistors (DUT) is high. It is in this frequency range where some components of the test setup may generate undesired reflections that overlap with the instability zone of the DUT.

This, long overdue, note describes typical causes for spurious oscillations in load pull setups and provides an overview of techniques, developed by Focus Microwaves, in order to prevent this from happening and protect the transistors during testing.



Typical Spectrum Analyzer screen shot during spurious oscillations at the output of a load pull set-up.

Causes for Spurious Oscillations

The basic fact to remember is that, while the Operator is focused on one or two test frequencies, the transistor itself does not know that. The transistor sees the whole setup over the entire frequency range and is subject to spurious oscillations, which start

from wideband background noise, as soon as the "oscillation conditions" are met at both test ports, source and load simultaneously.

Oscillation conditions are defined as the situation in which a passive load impedance creates negative impedances looking into the source port of the transistor and vice versa. Stability Circles are used to describe this phenomenon graphically: Stability Circles are the transforms of $|\Gamma_{Load}|=1$ to the Source side and $|\Gamma_{Source}|=1$ to the load side correspondingly.

As long as the Stability Circles enter into the Smith Chart area the transistor is potentially unstable, i.e.: there exist passive loads ($|\Gamma|<1$) for which it may oscillate (figure 1).

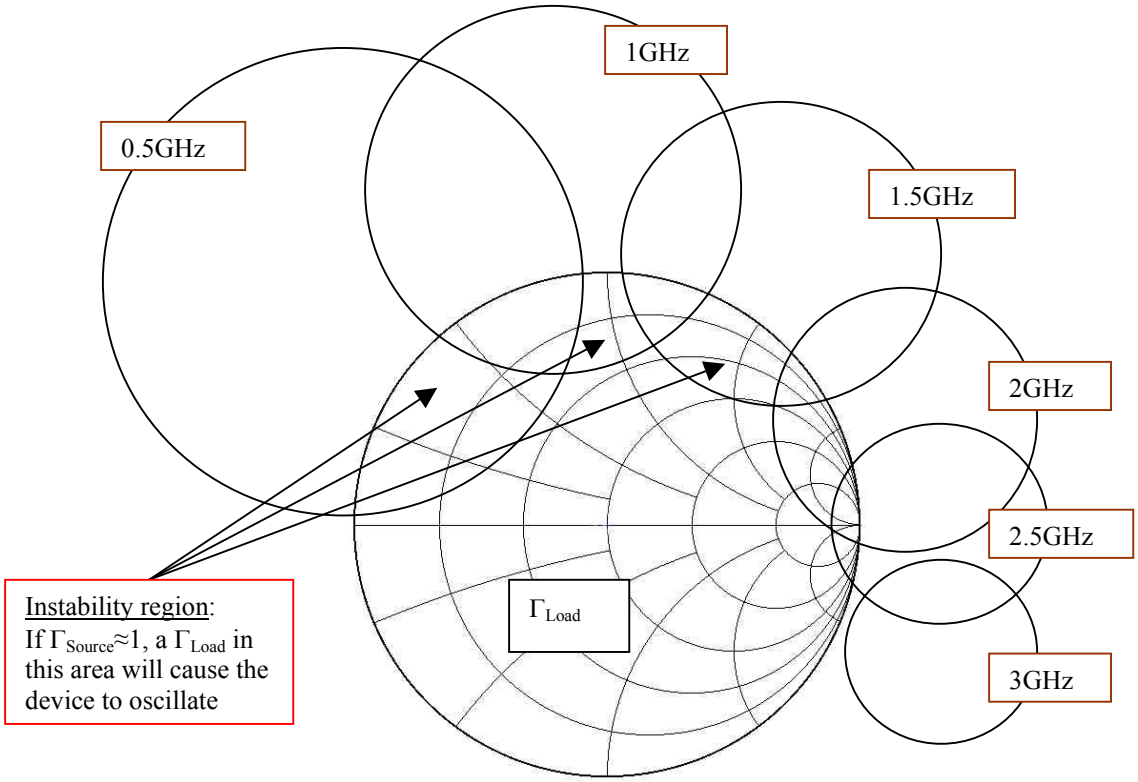


Figure 1: Typical Load Stability circles of a power transistor. This device is potentially unstable up to 2.5 GHz. Each circle corresponds to the image of the $|\Gamma_{Source}|=1$ circle at the corresponding frequency.

The first possible cause of spurious oscillations is, of course, the tuners themselves. Here we must distinguish between the different types of tuners used:

1. Electromechanical slide screw tuners, used by Focus and Maury, have, typically, a low-pass behavior; this means that the risk of spurious is low and, if they occur, then they appear close to the test frequency.

2. Electronic tuners (ex. ATN, called ETS by Maury Microwave and offered now also by ACCO USA) use switched pin diodes and create random reflections over a wide frequency range, including the MHZ region; this means that the risk of spurious is higher at low frequencies.
3. Mechanical multi-stab tuners, used typically in manual test set-ups, also create high reflection at low frequencies and may cause spurious in the MHz frequency region.

Other components of the set-up that may cause spurious oscillations are those with non-zero reflection factor over a wide frequency range, especially low frequencies, such as:

1. Bias Tees or Bias Networks on Fixture (if poorly designed)
2. Isolators / Circulators (critical outside their operation band)
3. Low loss Diplexers and Triplexers (in Harmonic L/P setups)
4. Poor or worn-out adapters and cables.

In the following sections we will discuss each item separately and means of possible improvement.

1. Bias Tees

Load Pull setups often require high power bias tees. The problem with such bias tees is that the inductances are laid out to carry 10 to 30A DC current and cannot be optimized to guarantee low reflection down to DC. Using a resistance parallel to the inductance will reduce the risk of oscillation (it reduces $|\Gamma|$), but it cannot be used on the Drain/Collector side of the DUT, since it would drain away too much current.

As a possible cure we should use two different bias tees, one low-current unit with a parallel resistor for the control port (Gate, Base) and one high-current unit for the output port (Drain, Collector).

Acceptable Return Loss is 15dB or higher down to very low frequencies. 10dB return loss can be accepted only at the high frequency end.

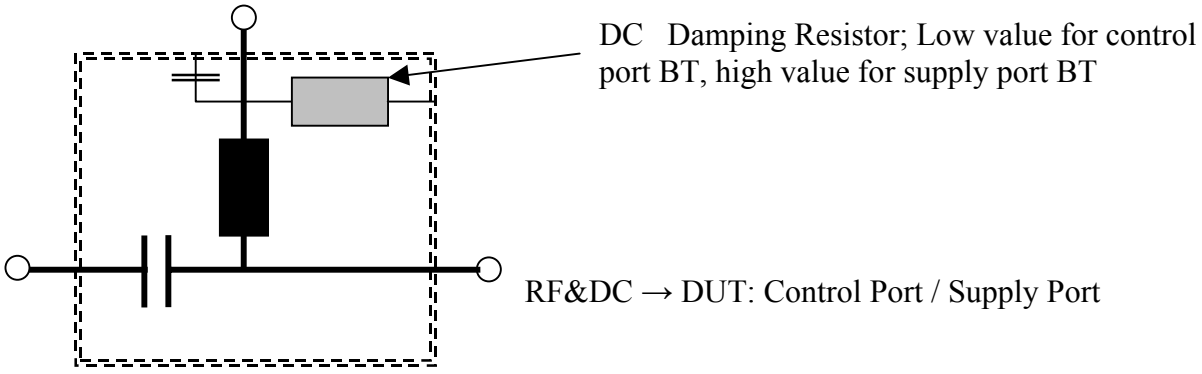


Figure 2: Typical high power Bias Tee

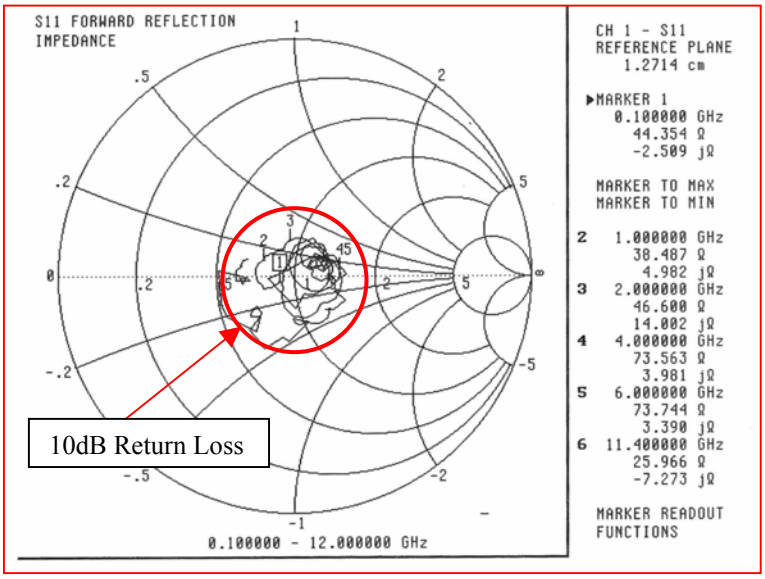


Figure 3: Typical S_{11} of Focus high power Bias Tee (30A, 50V DC).

2. Isolators (Circulators)

Isolators are useful in sensitive measurement setups because they effectively eliminate backflow of signal and multiple reflections and thus measurement uncertainties.

In load pull setups isolators are mandatory between the input coupler and the source tuner, in order to accurately measure the injected power; they eliminate signals reflected at the source tuner, which would falsify injected power readings, because of the limited input coupler's directivity.

Inside their pass band, isolators have low reflection (S_{11} and S_{22}) and inverse transmission (S_{12}) and almost unity forward transmission (S_{21}). In this frequency range there is no risk for spurious oscillations caused by the isolators. However, outside their pass band, isolators may create such parasitic oscillations. The reason is that in this frequency area, reflection factor of isolators can be high, beyond 0.5 or even 0.7 (Return Loss < 3dB).

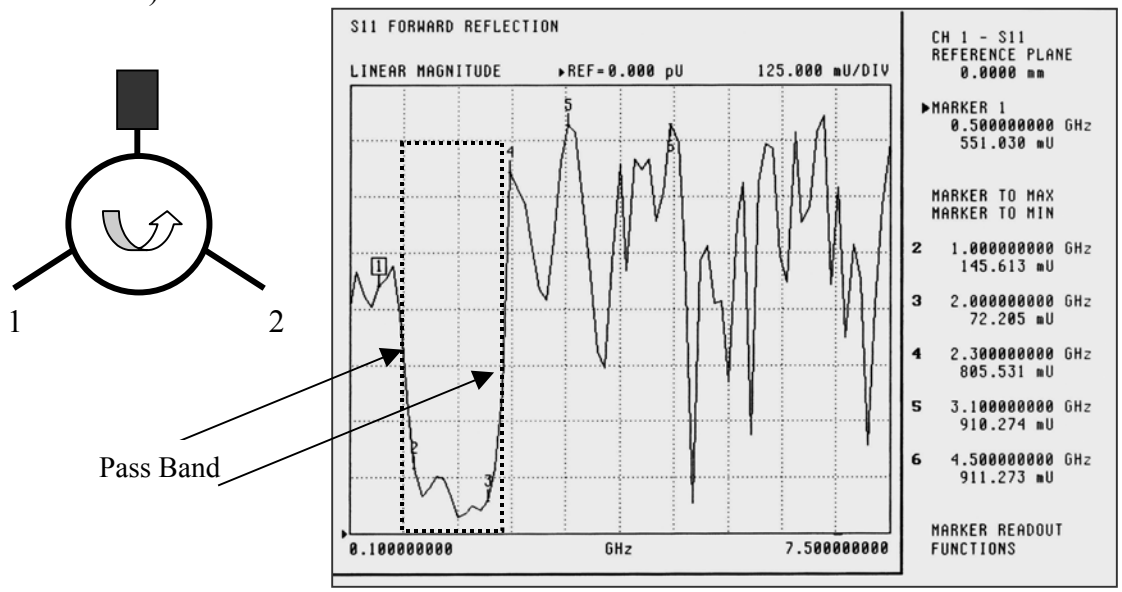


Figure 4: Wideband reflection behavior of 1-2 GHz isolator.

If a problem with spurious oscillations due to input isolator reflections (Γ, figure 4) in the setup occurs, the only remedy is to insert a low value (3dB) attenuator between isolator and input bias tee (figure 5). This will probably cure the spurious oscillations problem, but at the cost of increasing the driver amplifier power requirement by the amount of attenuation added.

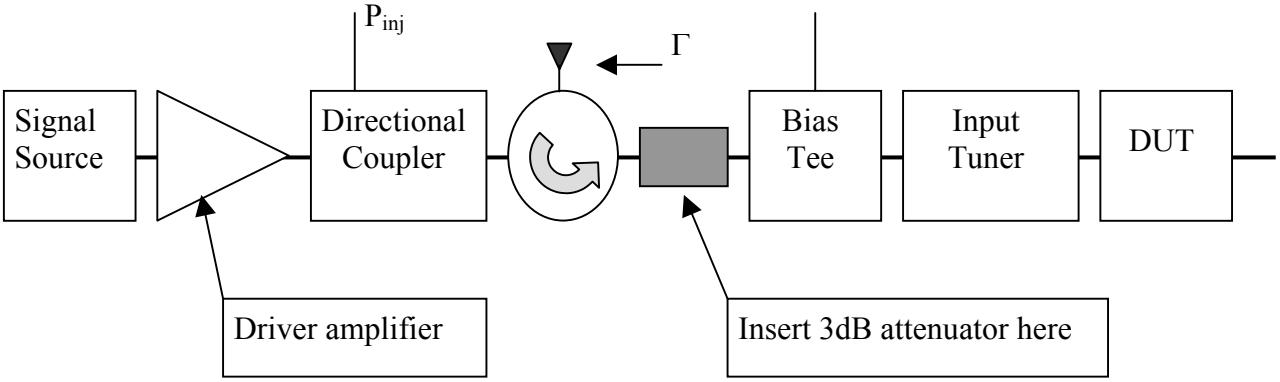


Figure 5: 3dB attenuator used to mask isolator "out-of-band" reflections.

3. Diplexers and Triplexers

Some harmonic load pull setups use Diplexers or Triplexers, in order to separate the signal from the harmonic frequencies and be able to control the corresponding reflection factors independently using different tuners, mounted in a "star" configuration (figure 6).

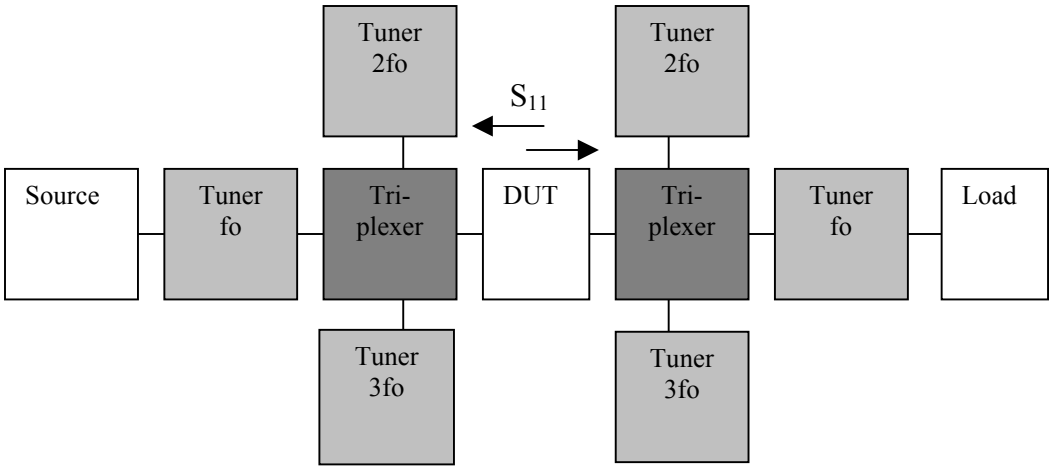


Figure 6: Harmonic Load Pull setup using Triplexers and tuners at the 3 harmonic frequencies

This setup is relatively easy to understand and employ, because it provides enough harmonic tuning isolation between the three frequencies fo, 2fo and 3fo generated by the DUT, when it is driven into its nonlinear operation range. If the insertion loss of the Triplexers and the associated reduction of effective tuning VSWR at DUT reference

plane can be tolerated [1], the remaining problem with this setup is spurious DUT oscillations.

The reason for this is the fact that most Triplexers are low loss – high (out-of-band) reflection components, in nature: They are made of star configurations of carefully tuned band-pass filters, which reflect all power outside their pass-band frequency range.

Reflection factors (S_{11}) at the DUT test ports, at frequencies outside the pass-band range, are typically >0.9, and, which is most annoying, this is the case also at the low frequency end, where the transistor gain is highest and the stability circles enter the Smith Chart (figure 1).

Figure 7 shows typical behavior of a state-of-the-art Triplexer, designed for and used in harmonic load pull setups [2].

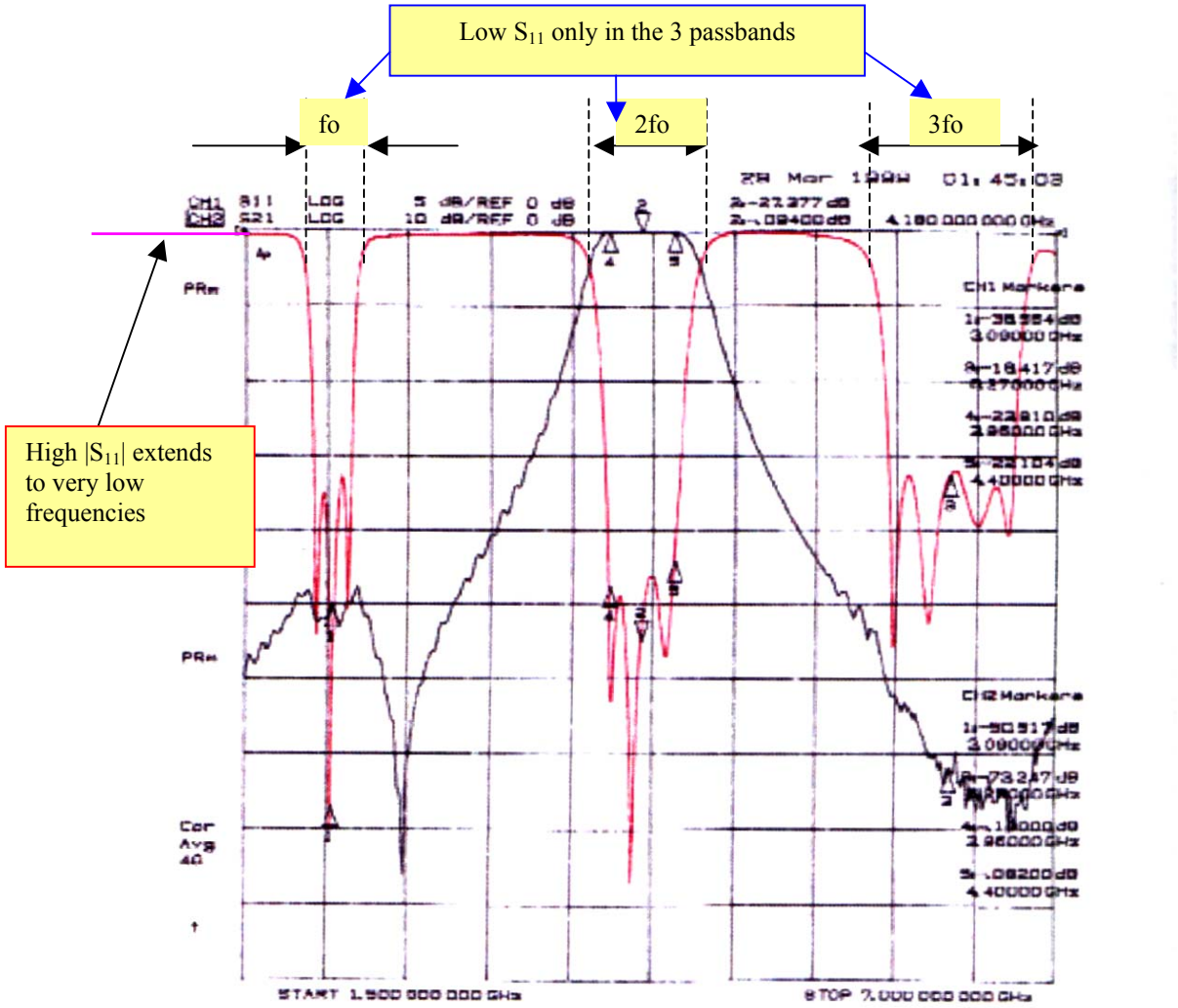


Figure 7: Wideband frequency response of Triplexer used in harmonic load pull setups. High S_{11} (≈1) outside the three pass-bands is obvious. When connected to the DUT the risk of overlapping with stability circles (figure 1) is obvious.

If two Triplexers of this kind are used in the harmonic load pull set-up for source and load tuning, spurious oscillations will in fact be probable. If only one Triplexer is used and the other test port is loaded with low VSWR, then it is possible that the transistor will not oscillate, but this must be evaluated on a case-by-case manner. In general, though, it can be said that this particular setup is prone to spurious oscillations.

4. Poor or worn-out adapters and cables

Bad cables and adapters are, unfortunately, a common phenomenon in microwave test labs. Adapters (even the expensive ones) and cables, even if handled properly (which is rarely the case), are consumable items that must be checked regularly and replaced. Bad test results originate, based on our experience, in more than 50% of the cases in such bad components. Besides bad results such components may cause spurious oscillations, if their return loss is worse than 10dB. Please do not chuckle; we have seen it too often in order not to mention it.

A very simple and good test for the integrity of cables and connections is to deform them slightly under observation of the wideband transmission (S_{21}) on a network analyzer. If the amplitude and phase of S_{21} change beyond a few hundred's of a dB or 0.5 degrees with mechanical deformation of the cables, then they need replacement. There is no point continuing calibrations and tests using these components.

Oscillation Detection and Protection during Load Pull

As discussed previously, spurious oscillations may occur before or during Load Pull testing. Most often (but not always) those oscillations occur at frequencies different than the test and its harmonic frequencies, where the source and load impedances interfere with the stability circles of the DUT's.

The occurrence of oscillations depends on the DC bias of the transistor, the tuner positions and, sometimes, on the input frequency and power. Even if spurious oscillations do not occur at the beginning of the testing and even if the tuner impedances themselves do not cause them, load pull affects the operation conditions (saturation, DC bias…) of the DUT and thus may change its stability behavior during the test itself and generate oscillating conditions. As previously mentioned, spurious oscillations falsify the test result and may cause destructive failure of the transistor.

The false results normally become visible in 3D load pull surfaces and may be corrected by eliminating "bad" points using automatic or manual numeric 'filters' in the *WinGraph* or *ContourViewer* contouring program.

Oscillation Detection

In order to avoid, possibly destructive, oscillations in high power transistors, due to the tuner impedances (↔mechanical tuner positions) Focus software provides an option called "Oscillation Detection".

The "Oscillation Detection" procedure uses a number of techniques in order to automatically identify, during Load Pull, at which tuner positions the DUT oscillates (at any frequency). This is accomplished as follows:

- Spurious (non harmonic) signals are detected using a Spectrum Analyzer (fig.8).
- DC current exceeding user-defined limits is detected.
- Power added Efficiency (PAE > 100%) is detected.
- Gain > Max (user defined) is detected.

Typically one of the above events will occur if the transistor oscillates. If it oscillates at frequencies other than the test frequency (and its harmonics), the spurious oscillations will be detected through the spectrum analyzer. If it oscillates at the test frequency (like a synchronized oscillator) typically the gain or PAE will exceed the user defined limits, because the output RF power will be much higher than the injected power.

When one of the above events occurs, the corresponding tuner position is saved in a special file in the default directory. This file is then used, when the option "Oscillation Protection" is activated, in order to steer the tuner away from these positions, thus avoiding spurious oscillations. If the oscillations are really spurious, thus not related to the test frequency, as is often the case, then the information contained in this file can be used at other test frequencies too, in fact protecting the transistor.

Further-on spurious DUT oscillations can be avoided if the test is carried out only in a limited area of the Smith chart (figure 11). This area can be defined in the Focus software either in the form of a rectangle, a segment or a user defined selection of points (pattern). This area is defined precisely in order to avoid impedance areas where the transistor might oscillate. Combining such a limited area with the techniques described in the next section create a very effective tool of oscillation protection of the DUT's.

Transient Oscillations

It often happens that the DUT oscillates at tuner positions different than measurement points, which are, typically, tuner calibration points. In this case neither of the above tests will detect this oscillation, because the tests are done when the tuner "rests" at a measurement point. In this case there is no point detecting and remembering the wrong tuner positions. Transient oscillations occur, because the tuners move horizontally between load pull points with the probe inserted deep into the transmission line, i.e. at constant, rather high, VSWR.

A special routine is available in the Focus software, which retracts the probe from the Slabline during horizontal tuner movement and re-inserts it when it reaches the next test point. This technique is called "Probe Sampling" and has saved quite a few transistors from destruction (figures 8 and 9). The only disadvantage of this technique is the increased test time, due to the vertical probe movement.

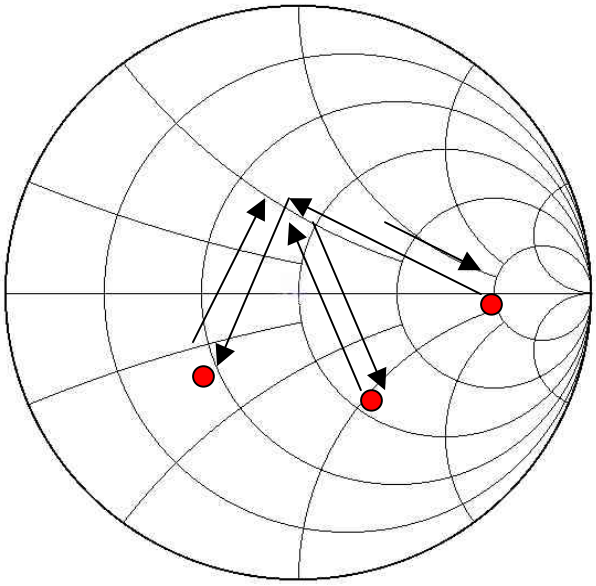


Figure 8: Probe and reflection factor movement during load pull with "Probe Sampling". The arrows show the trace of the reflection factor of the tuner between successive calibration points, turning clockwise.

Another technique, also available in Focus' software is "Power Sampling". In this case the user may select to reduce the signal power by a number of dB (typically 10 dB) after the measurement is finished and just before the tuner moves and restore it after the tuner stops, in time for the next measurement. This way the device is staying "cold" during the tuner movement (figure 10).

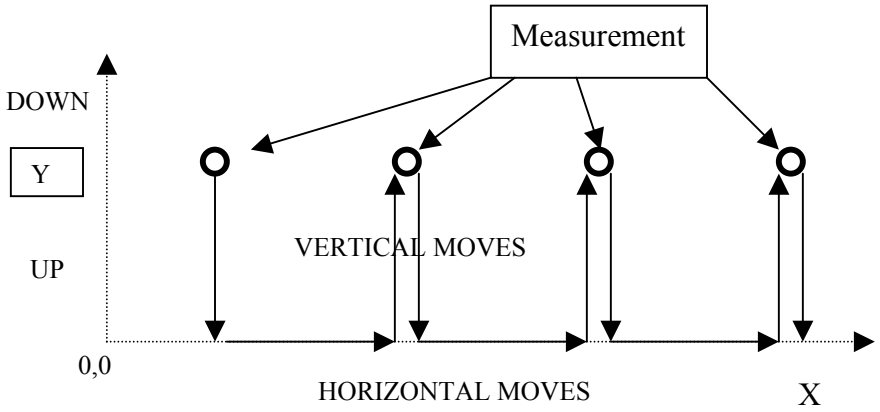


Figure 9: Probe movements during "Probe Sampling".

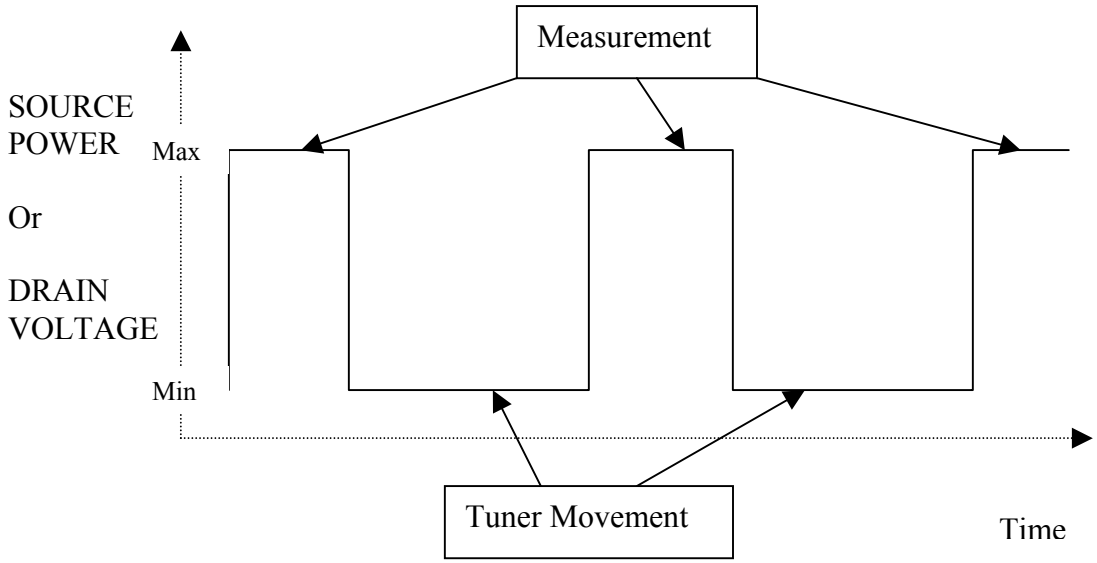


Figure 10: DC Bias and RF power injection during tuner movement and "Power or DC Sampling".

The last technique used, in order to prevent catastrophic DUT failure, is "Supply Voltage Sampling", in which case, again, as in "Power Sampling" the supply voltage on port 2 of the DUT is reduced to a user defined value during the tuner movement and restored to the nominal values during the measurement (figure 10).

All these techniques and their combined application help reduce the risk both of false measurements and device failure due to parasitic oscillations during automatic load pull. More information about these techniques is also available in Focus' Application Note 23 "Selective Load Pull using pattern and section tuning", summarized here in figure 11.

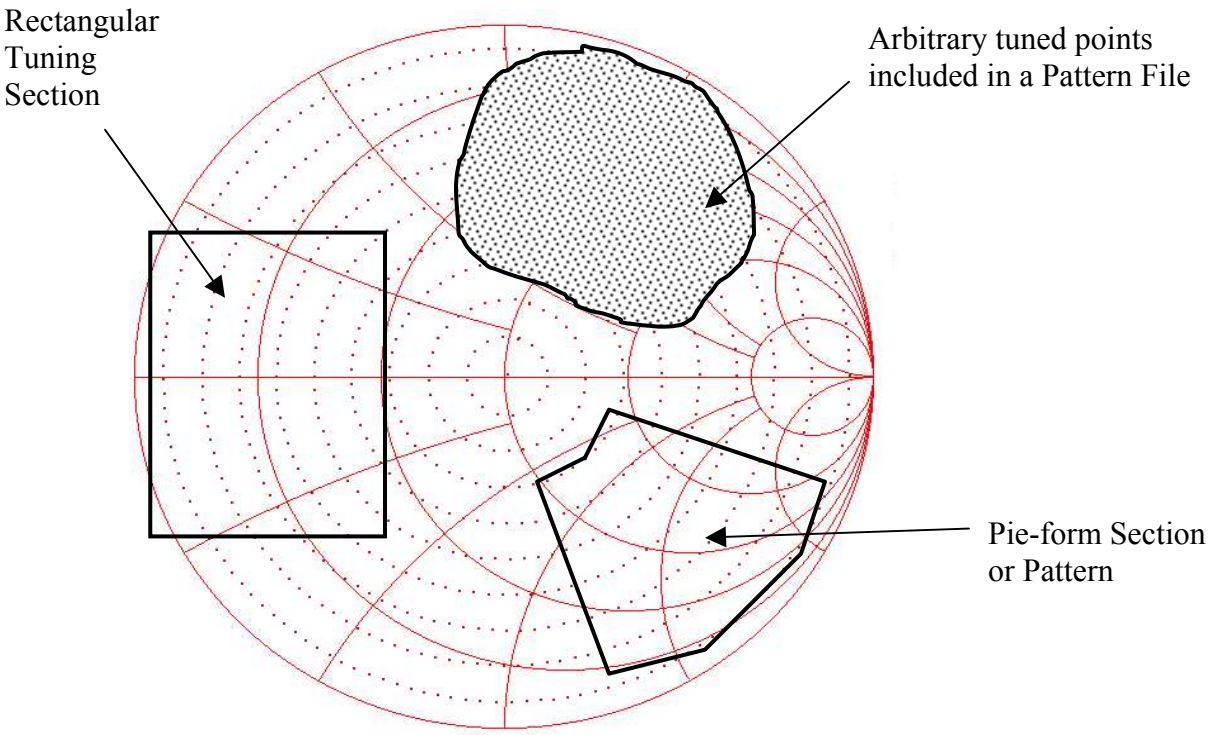


Figure 11: Typical Section and pattern tuning for selective load pull available in Focus Software