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Application Note No 11

Load Pull Measurements on Transistors with Harmonic Impedance Control

Multi Harmonic load pull improves the Power Efficiency of Transistor (Bipolar and FET) power amplifiers. The increase in efficiency may reach 10-12% in FET and 7-8% in Bipolar Transistor amplifiers.

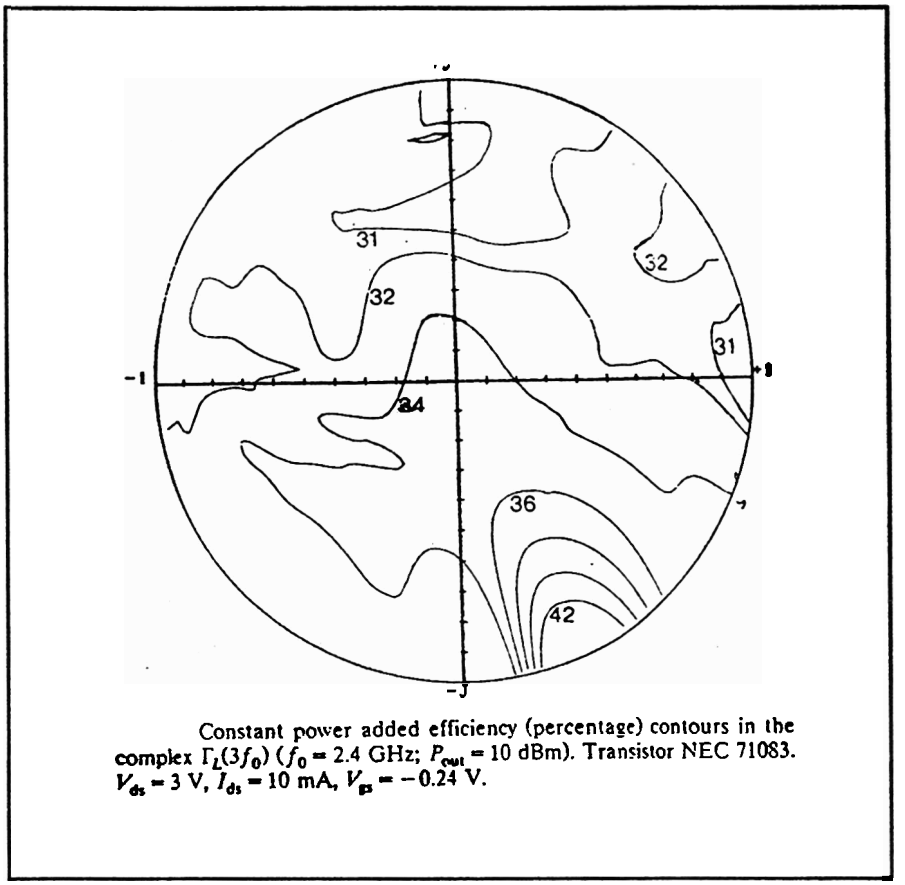
This note describes a simple technique to be used Focus Microwaves' pre-calibrated programmable Tuners for Load Pulling Power Transistors at the fundamental and simultaneously control the load impedances at the different harmonic frequencies.

Introduction

The work done at Ecole Polytechnique de Montréal [1] and elsewhere, demonstrates that the efficiency of FET power amplifiers can be increased by tuning the third-harmonic impedance at fixed fundamental and second-harmonic impedances for a given output power. In the case of the NEC 71083 MESFET used as a class AB amplifier, the efficiency could be improved by about 10 % by tuning the third harmonic load (figure 1.)

In general power efficiency can be improved by placing a **short circuit** with a **specific phase** at the third-harmonic at the output of the transistor. However this particular phase needs to be experimentally determined. This note describes a simple technique to determine this phase for a specific frequency.

Dependence of Transistor Efficiency on 3rd Harmonic Load [1]



Constant power added efficiency (percentage) contours in the complex $\Gamma_L(3f_0)$ (f_0 = 2.4 GHz; P_{out} = 10 dBm). Transistor NEC 71083. V_{ds} = 3 V, I_{ds} = 10 mA, V_{gs} = −0.24 V.

Figure 1: Multi Harmonic Load Pull on GaAs FETs

Load Pull Setup

The measurement setup used for this application is shown in figure 2.
It utilizes a synthesized signal source (S1), an input coupler (C1), two programmable pre-calibrated tuners (T1 and T2), a microstrip test fixture (TF, in our case the Focus Microwaves power transistor fixture, model PTJ-0, figure 2) and a dual channel power meter, together with some bias tees, isolators and attenuators.
The setup is completely controlled by an IBM®-PC compatible computer with GPIB and tuner control interface, as supplied by Focus Microwaves.
For Intermod measurements a second source has to be added at the input and the output to be connected to a spectrum analyzer.

In normal operation this setup can measure and optimize Output Power, Gain and Efficiency of any device mounted in the test fixture as a function of source and load impedance. Source/Load Impedance values of a few Ohms (in 50 Ω system) or a few tenths of an Ohm (in a transforming test fixture) can typically be synthesized by the tuners [2], all at the fundamental frequency of operation [3].

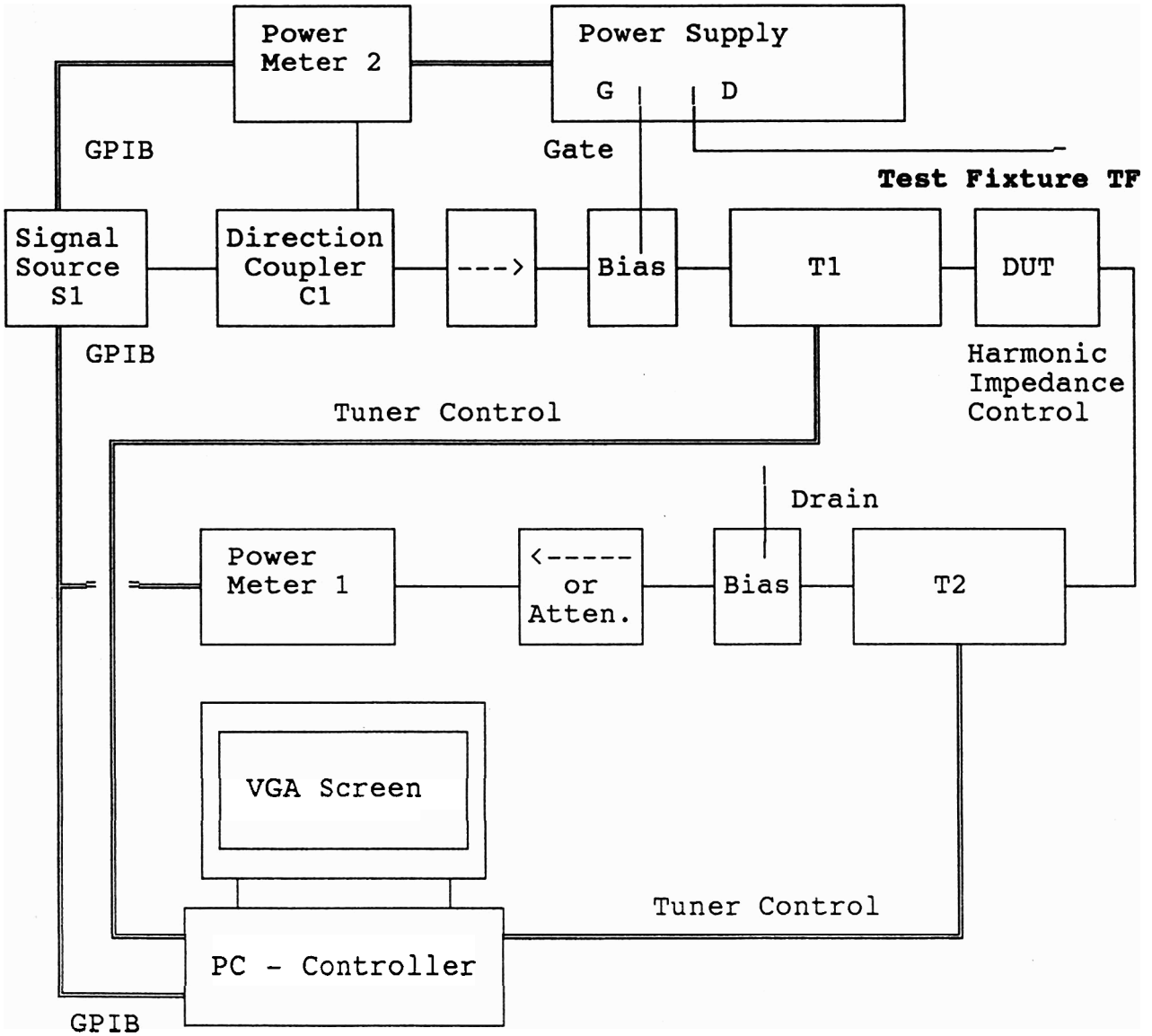


Figure 2: Load Pull Setup for Power, Gain, Efficiency with Harmonic Impedance Control

The particularity of this setup consists in the specific layout of the output microstrip network of the test fixture. which is a modified version of the standard PTJ-0 (figure 3). This network includes a number of open stubs that can be connected to the main line at given offset phases, as shown in figure 4.

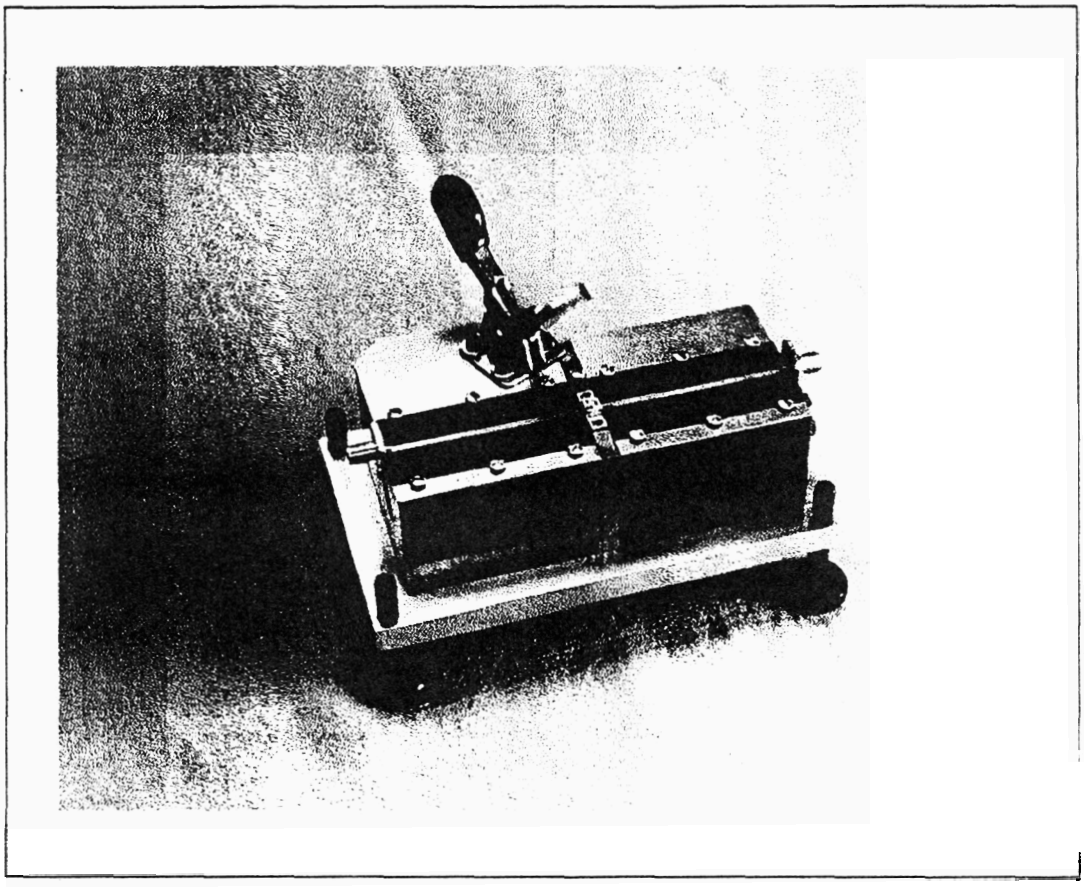


Figure 3: The Power Transistor Test Fixture. model PTJ-0.

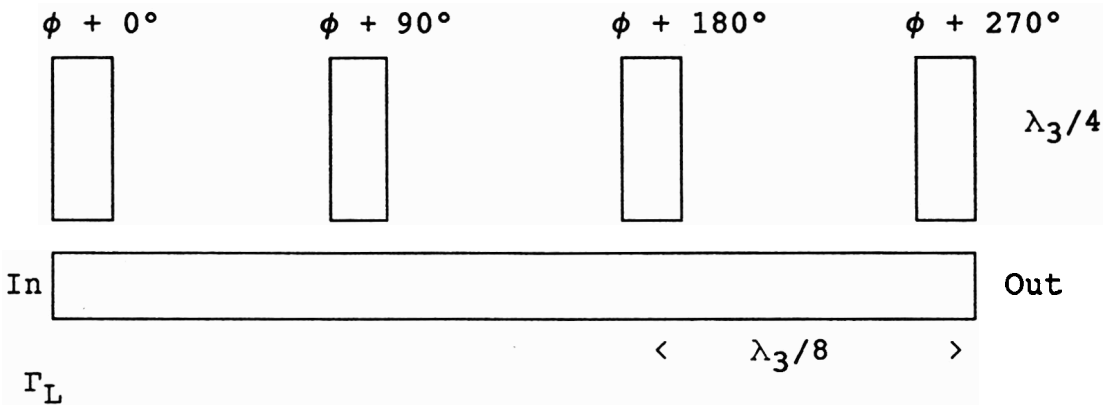
Determination Optimum Phase of Load

In order to determine the optimum phase of the short circuit to be connected at the output of the transistor at the 3rd harmonic the following measurements need to be effectuated:

1- Search. using the fundamental load tuner the optimum load for maximum Power Efficiency.

2- Add to the transmission line of the test fixture (before the tuner) an **offset phase network** (figure 4). This is a set of four 90° offset shorts (λ /4 open microstrip lines at the third harmonic frequency).
Connecting one short after the other and measuring the power efficiency provides enough information to find the required optimum phase at $3*f_0$.

The optimum phase will not necessarily correspond to one of the selected phases, but the shape of the response always permits to determine the exact phase by interpolation (figure 5).



λ_1 = Wave length at the Fundamental frequency
λ_3 = Wave length at the Third-Harmonic frequency
$\lambda_3 = \lambda_1/3$

Figure 4: Harmonic Impedance Control Network, to be placed at the output side on the test fixture

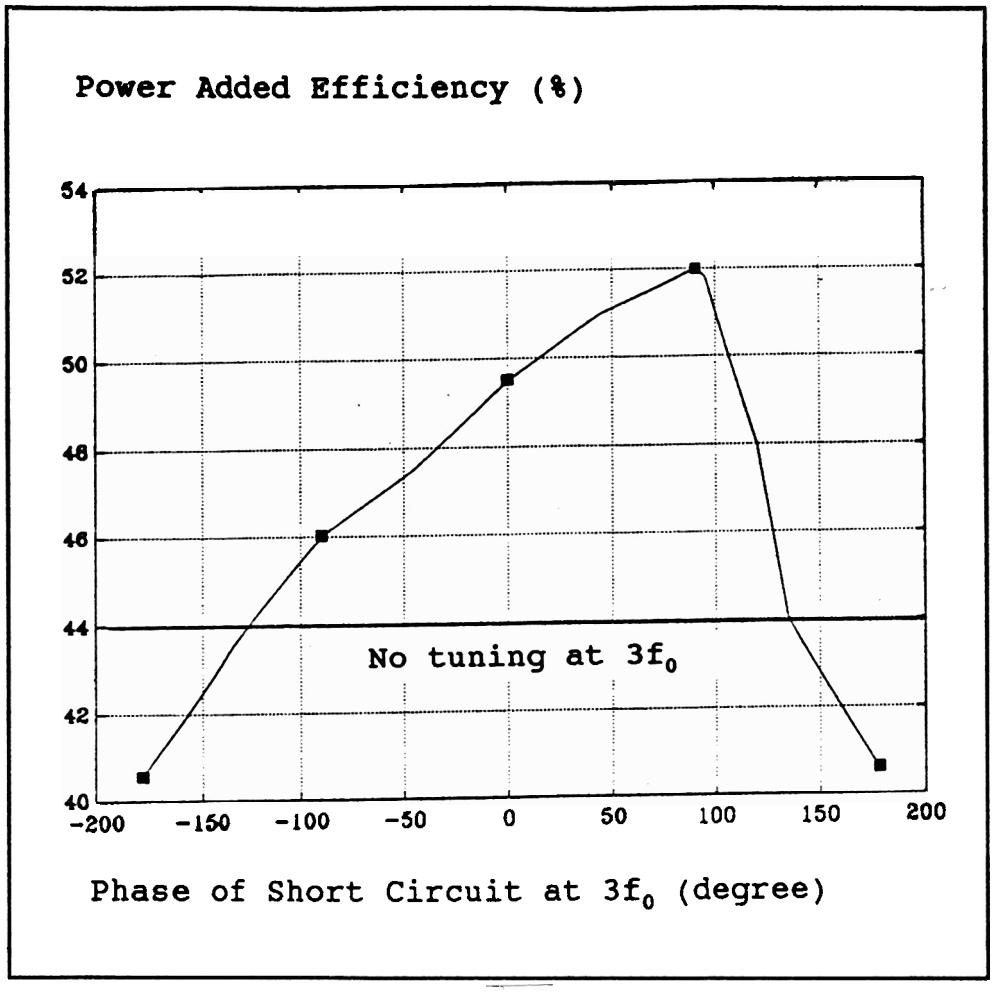


Figure 5: Dependence of Efficiency on Phase of Harmonic Short

For a finer resolution the network can be enhanced by adding open stubs at the opposite side of the microstrip and 45° off phase.

Conclusion

Full Harmonic Load Pull Setups [1] can provide very useful information about the nonlinear behaviour of transistors, but for the design of a high efficiency power amplifier this kind of setup requires too must time, money, a lot of specific instruments and people for to be cost effective.

The uncomplicated technique described in this Note uses a simple microstrip circuit as part of the test fixture combined and a pre-calibrated 'of the shelf' load pull tuner system and permits to optimize the 3rd harmonic load for optimum power efficiency of FET and bipolar transistor amplifiers.

References

[1] Ghannouchi et al. "A Multi Harmonic loading method for large-signal microwave and millimetre-wave transistor characterization", IEEE Transactions on microwave theory and techniques, Vol.39 (1991) No. 6, pp. 986-992

[2] Application Note No 6, "Load Pull Measurements on Very Low Impedance Transistors", Focus Microwaves, 1993

[3] "Low Cost RF Tuner System for JDC Load Pull and SSPA Design", Focus Microwaves, paper presented at RF Expo East, 1993