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***Application Note 7***

# Load Pull of Potentially Unstable Transistors

The CCMT system supports a variety of techniques that allow to determine and avoid impedances at which the transistor under test oscillates. Oscillations may be detected either by registering increases of gate or base currents or by detecting spurious signals using a spectrum analyzer. The oscillating points are registered in a file and are automatically eliminated from further load pull tests at the same frequency.

## Introduction

Parasitic Oscillations during automatic Load/Source Pull measurements are an annoying phenomenon that may significantly falsify the measurement and eventually destroy the transistor under test. The CCMT system supports a number of techniques, which can be used to avoid this:

• The User can define a **rectangular or "pie" Segment** of the Smith Chart where he does not want the tuner to tune to, if he knows the dangerous areas before the test.

• Alternatively he may define an **Impedance Pattern** using Mouse tuning and make load pull measurements only on those impedances, again knowing ahead of time where there is no problem to tune to.

Both techniques presume an intimate knowledge of the transistor's behaviour.
An automatic system should though be able to detect oscillations automatically, save documented information on the conditions which caused them and be able to use this information at a successive test, in order to automatically avoid those points.

There are three possibilities for this latter task: 1) Detecting the gate (or base) current generated by a self-detection of the oscillation; 2) scan the broadband response of a spectrum analyzer or 3) detect the change of the output power.
This note describes the automatic techniques 2) and 3). The User defined section and pattern operations are described in Application Note 16.

# Load Pull Setup for Potentially Unstable Transistors

Figure 1 shows the load pull setup used which permits to minimize the risk of and detect and avoid the impedances, which cause parasitic oscillations. The 3dB attenuator between the input isolator and bias tee serves to reduce the reflection factor presented to the DUT input at frequencies outside the frequency band of the isolator. These reflections may be quite significant (of the order of 0.5 or more), in other words, an isolator is not the safest way to avoid parasitic oscillations.

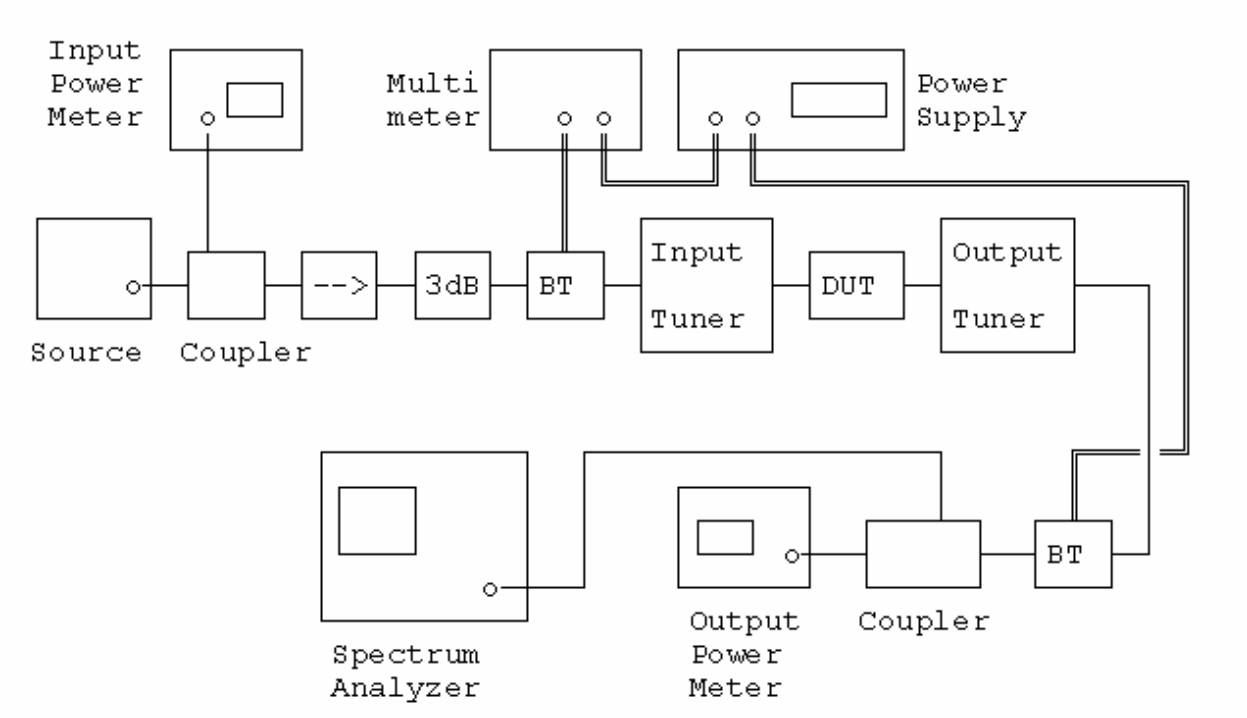


**Figure 1: Load Pull setup allowing the detection of parasitic oscillations**

When a parasitic oscillation occurs three things happen, in general:

1- The DC bias changes suddenly.
2- Spurious signals appear at the output of the DUT.
3- The output power surges abruptly.

The internal oscillation is, in the case of a FET, detected by the gate electrode, which causes a steep increase in gate current.

It is difficult to define and detect changes of the output current, since those changes may vary between 1 and 50% this depending very much on the load impedance at the frequency of oscillation. The change in gate bias is always distinct because the gate current under normal conditions is nearly 0. It is very difficult to design an algorithm that would safely detect changes

of 1 or 2% of drain (collector) current and decide if this is an oscillation, since those changes may well be due to the changes of load impedance during load pull but without the presence of an oscillation.

Reading the spectrum analyzer may also critical. As long as the parasitic oscillations occur at frequencies different than the operation frequency and its harmonics, detecting the spurious on the spectrum analyzer would be easy. If, however, oscillations occur at the operation frequency or its harmonics, designing a measurement algorithm that detects them safely is practically impossible using the spectrum analyzer. In this case a further technique may be used: To detect the change of the output power level as a function of load impedance and trigger an "oscillation detection" routine if this change exceeds a User defined value.

CCMT uses a combined technique in order to detect parasitic oscillations:

a) An fast 8 bit AD converter that detects gate current before each measurement. This converter is included in Focus' AB08 PC interface card.
b) A routine that reads a (user defined) broadband spectrum analyzer and detects parasitic oscillations.

Both techniques can be activated simultaneously or individually.

1- Use a digital multi-meter (in addition to the analog interface) to detect a gate current as indication of self-detected oscillations.
2- Use a spectrum analyzer coupled at the output to detect spurious oscillations.
3- Register the corresponding impedances in a file for later consideration.
4- Optionally ignore these impedances or set the measured values at a distinct level for easy recognition when processed in 3D plots.

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in the spectrum method we cannot detect oscillations at the operation frequency itself, neither at the harmonics
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