MM-Wave Noise Characterization of 40nm CMOS Transistor for up to 67 GHz

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***Abstract* — This noise modelling, characterization and measurement from 0.5 GHz to 67 GHz is reported for the first time in coaxial. RF CMOS devices fabricated on GLOBALFOUNDRIES' 40nm technology are measured with Focus Microwaves noise system for full frequency span of 67 GHz. Experimental results agree well with theoretical and modeling results.**

***Index Terms* — CMOS technology, millimeter wave transistors, noise measurement, semiconductor device modeling, thermal noise, tuners.**

I. INTRODUCTION

High frequency noise is an increasingly important issue in RF IC (Radio Frequency Integrated Circuits) design as market demand for faster wireless communication product pushes CMOS devices to operate at mm-wave frequency regime (>60GHz). Further, increasing integration density of transistors has caused surge in overall generated noise power in RFICs and noise immunity is deteriorated as power supply of CMOS devices continues to reduce along the device scaling trend. Thus, there is a strong need to accurately characterize the high frequency noise behavior of CMOS transistors to assist IC designers in verifying the noise performance of the circuit designed prior to fabrication. In order to ensure high quality of HF CMOS noise model developed, accurate and precision noise measurement data is needed.

Noise measurement at mm-wave frequencies is a great challenge as the gain of device diminishes. Under such circumstance, noise receiver with extreme high sensitivity (high gain, lowest possible noise figure) is required for reliable noise measurement. Particularly, robust noise measurement of advanced CMOS devices (40nm and beyond) is becoming critical as its minimum noise figure, NFmin approach closer to uncertainty limit of instrument (0.2dB [1]). This is further exacerbated by increasing mismatch in input impedances due to higher gate resistances [2], [3]. Traditional noise parameter extraction techniques rely on the measurement of noise figure at several impedance points and a least square fitted solution based on algebraic decomposition of the basic noise parameter formula [4]. However, given current generation sub-nm CMOS devices, traditional techniques are no longer sufficient because can fail due to measurement inaccuracies, as is common with CMOS devices with very low noise figure and high reflection coefficient. Additionally, the practical use of traditional techniques is limited when trying to extract noise parameters over a wide frequency range.

Our solution is to perform a new type of impedance pattern distribution, as well as a statistical extraction technique that is based on combinations of appropriately selected impedances. Specifically, three sets of impedances are generated, which are optimized for the lowest, middle, and highest frequencies. This ensures that there will always be appropriate subset of noise parameter data for extraction on each frequency in a sweep. The statistical extraction then selects an appropriate subset, per frequency, of the total noise figure measurements. These points are then used to perform millions of extraction using different combinations of the selected data. The resulting extractions are then statistically analyzed to produce a final set of noise parameter data over frequency.

The proposed solution offers several advantages. First, it produces viable noise parameter extractions even with extremely difficult to measurement 40-nm CMOS devices. Secondly, the tolerance of the system to measurement errors is dramatically improved. Under such circumstances, traditional methods are unable to produce any results. Finally, the method fully utilizes the high speed, sweep based data acquisition that is possible using the current generation noise figure measurement hardware.

In this paper, 67GHz thermal noise measurement of 40nm CMOS device is presented for the first time. The device technology and the proposed noise extraction technique are detailed in Section II and III respectively. In Section IV, experimental validation of measured noise data is discussed.

II. GLOBAL FOUNDRIES: TRANSISTOR TECHNOLOGY AND CHARACTERIZATION

A. Technology

The devices reported in this paper are fabricated on GLOBALFOUNDRIES' 40nm technology where multi-

finger style of layout is used for optimum RF performance. Besides that, the device gate terminals are contacted at both ends to ensure low gate resistance. Meanwhile, the body of the transistor is tied to substrate through surrounding guard ring.

B. Characterization

The noise behavior of the CMOS transistor described is characterized by GLOBALFOUNDRIES' 40LP RF/mm-wave thermal noise model. It is developed based on widely adopted BSIM4 holistic thermal noise model that has been known to be accurate at RF frequencies [5]. This is contributed by improvement in the channel thermal noise model to account for the amplification impact of transconductances, induced-gate noise and their correlation. Further, both short-channel effects and velocity saturation effect are addressed for modeling of advanced CMOS devices. The intrinsic gate resistance, non-quasi-static (NQS) effect and substrate resistance effect are enabled using the BSIM4 built-in gate resistance and substrate resistance models (rgatemod=3, rbodymod=1) with the model parameters adjusted to fit to the measured hardware data.

III. FOCUS MICROWAVES: NOISE EXTRACTION TECHNIQUE

Figure 1 illustrates a measurement setup used to extract noise parameters of a Device Under Test (DUT). The vector network analyzer (VNA) measures scattering

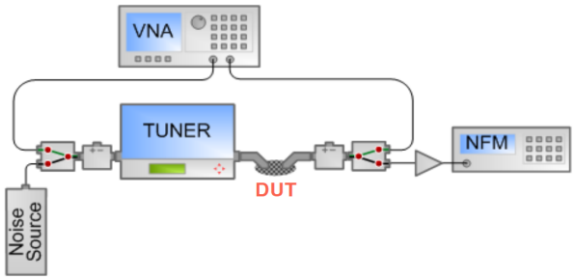


Figure. 1. Noise measurement setup. VNA: Vector Network Analyzer, NFM: Noise Figure Measurement, Tuner: Electromechanical tuner. Equipment from left to right: Noise source, switch, bias-tee, Tuner, DUT, bias-tee, switch, low noise amplifier (LNA), NFM.

parameters ([S]) of the DUT while the noise figure analyzer (NFA) measures total noise power (P_n) of the system including the DUT. The total noise factor of the system of Figure 1 is computed as follows:

$$F_{TOT}(\Gamma_s) = \frac{P_n}{T_0 kBG}\frac{|1-S_{11}\Gamma|^2|1-\Gamma_{Rx}\Gamma_s|^2}{(1-|\Gamma|^2)|S_{21}|^2} - \frac{T_C}{T_0} + 1 \quad (1)$$

In Eq. 1, S_{11}, S_{21} are [S] of the DUT, Γ_S is the source reflection coefficient seen by the DUT, Γ is the source reflection coefficient seen by the LNA, Γ_{Rx} is the input reflection coefficient of the LNA, T_c andT_0 are the actual and standard temperature (290K), respectively. The term kBG is the gain-bandwidth constant of the receiver and is given as:

$$kBG = \frac{P_H - P_C}{T_H - T_C}(|1-\Gamma_{Rx}\Gamma_s|^2)\left(\frac{|1-S_{11}\Gamma_{NS}|^2}{(1-|\Gamma_{NS}|^2)|S_{21}|^2}\right) \quad (2)$$

with $T_H = T_0\left(1+10^{\frac{ENR}{10}}\right)$ is the hot noise source temperature, ENR is the excess noise ratio of the noise source, measured in dB. Γ_{NS} is the reflection coefficient of the noise source in OFF state. The term kBG is computed by measuring the noise power density in two different states of the noise source: state 1) the noise source is ON (P_H, T_H) and state 2) the noise source is OFF (P_C, T_C). Once the total noise factor is known, the noise factor of the DUT is given as [6, 7]:

$$F_{DUT}(\Gamma_s) = F_{TOT} - \frac{F_{Rx}(\Gamma_s) - G_{OUT}}{G_{DUT}\, G_{OUT}} \quad (3)$$

where G_{DUT} and G_{OUT} are DUT's available gain and total available gain (loss) of the output network (bias-tee and switch), respectively. The noise factor of the DUT as a

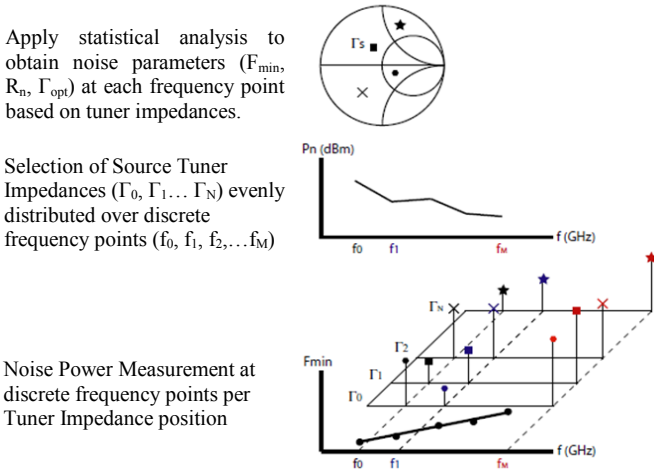


Figure. 2. Summary of noise extraction technique.

function of impedance presented by the tuner Γ_s is represented by:

$$F_{DUT}(\Gamma_s) = F_{min} + \frac{4R_n}{Z_0}\left(\frac{|\Gamma_{opt} - \Gamma_s|}{|1-\Gamma_{opt}|^2(1-|\Gamma_s|^2)}\right) \quad (4)$$

Where F_{min} is the minimum noise factor of the DUT, Γ_{opt} is the optimum impedance that result in F_{min}, and R_n is the equivalent noise resistance. Together, F_{min}, Γ_{opt} (amplitude and phase), and R_n is referred to as the four (4)

noise parameters of the DUT. Four measurements at non-overlapping source impedances are performed to obtain four linearly independent equations that are used to solve for the DUT noise parameters at a given frequency point.

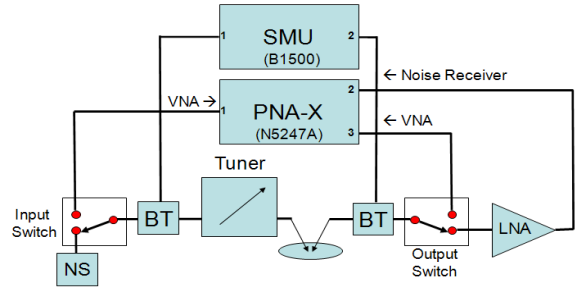
Figure 2 summarizes the noise extraction technique over wide discrete frequency points. Due to measurement errors, more than four tuner impedance states Γ_s (s = 0, 1, 2, ... N where N > 4) are commonly used to in measurement. Statistical analysis is subsequently applied to produce noise parameters data.

IV. CMOS TRANSISTOR NOISE MEASUREMENT AND VALIDATION

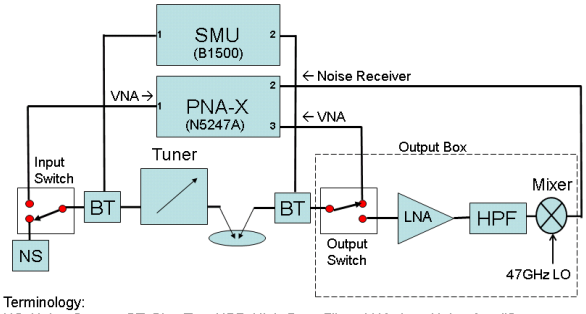
In this section, experimental validation of CMOS transistor noise measurements on GLOBALFOUNDRIES' 40LP RF/mm-wave thermal noise model is discussed.

A. Measurement Setup

The system setup for 10GHz-50GHz and 50GHz-67GHz noise measurements are summarized in Figure 3(a) and Figure 3(b) respectively. In both setups, HF noise and S-parameter measurements are performed by N5247A PNA-X (Nonlinear Vector Network Analyzer) under varying source admittances exhibited by Focus electromechanical tuners. The entire system is placed in the shield room to isolate from surrounding interferences. In addition to PNA-X noise receiver, external LNAs are connected at the DUT output to boost the receiver sensitivity and minimize noise measurement uncertainties. Three external LNAs with best optimized gain and noise performance are used for full coverage of the entire noise measurement frequency range (0.5GHz-26.5GHz, 26.5GHz-50GHz and 50-67GHz). Particularly, the 50GHz-67GHz LNA is connected in conjunction with RF high pass filter and 47GHz downconverter for downcoversion of HF noise signal to match the operation



(a)



(b)

Figure. 3. (a) 10GHz-50GHz noise measurement setup. (b) 50GHz-67GHz noise measurement setup.

frequency range of 50GHz PNA-X noise receiver. Meanwhile, the DC biasing conditions of transistor at input and output terminals are provided by Agilent B1500 Source Measurement Unit (SMU). Prior to any measurements, both noise and S-parameters calibrations are performed to establish measurement reference plane at probe tips using "Cold Source [8]" method and LRRM [9] technique respectively. The measured data is further processed by OPEN-SHORT [10] noise de-embedding algorithm to remove unwanted parasitic effects of pad and metal interconnects for up to Metal2 (M2) level.

B. Results and Comparisons

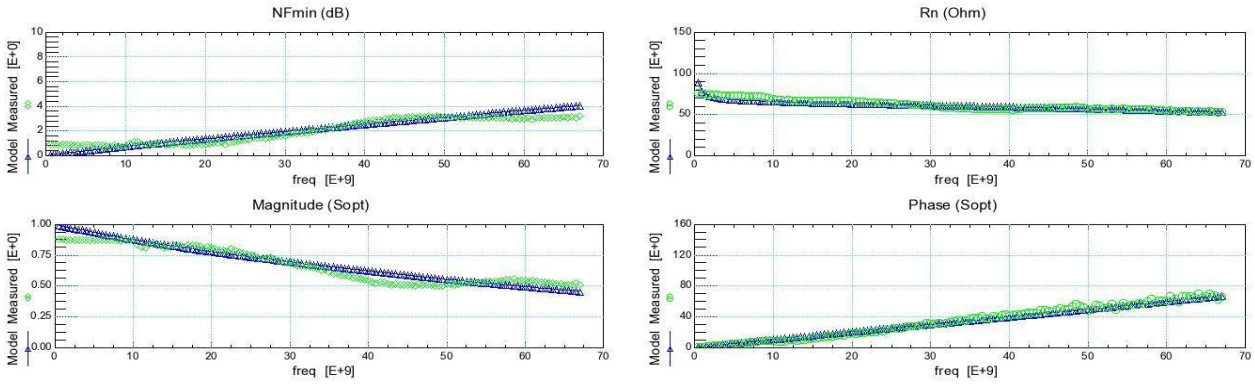


Figure. 4. Measured and simulated thermal noise parameters (NFmin, Rn, magnitude and phase of Sopt) of 40nm NMOS device of L=40nm, W_T=72um at Vgs=Vds=1.1V.

As part of the verification step, the correlation between measured noise parameters of 40nm NMOS device (Width Total, W_T=60um) after de-embedding and simulation result is investigated. Particularly, the transistor figure of merit, minimum noise figure, NFmin is considered as one of the critical parameters in LNA design. As shown in Figure 4, all de-embedded noise parameters of the CMOS transistor reasonably agree with the model for entire frequency span of 67GHz. The de-embedded measurement data is further validated on the frequency dependency of the channel noise power spectral density, S_{id}. It could be calculated from both noise and Y-parameters by: $S_{id} = 4kTR_n|Y_{21}|^2$. Theoretically, the channel noise power spectral density of CMOS device should exhibit constant behaviour across GHz frequencies since it is dominated by white noise. Figure 5(a)-(c) shows the comparison of de-embedded and simulated channel noise spectral density of CMOS transistor across different channel lengths (L) and total width geometries (W_T).

Overall, the de-embedded Sid of the transistor devices match theoretical prediction since it is relatively constant at measurement frequency range of 0.5GHz to 67GHz. The comparison results also suggest that the measurement data is scalable across device of arbitrary width and channel length geometries since good correlation between

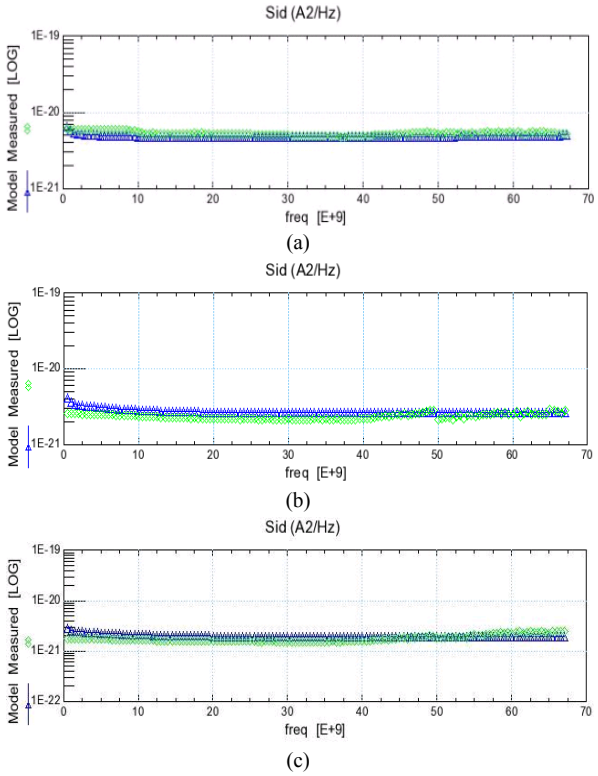


Figure. 5. Measured and simulated drain current noise density, S_{id} of NMOS devices: (a) L=40nm, W_T=60um (b) L=80nm, W_T=72um and (c) L=120nm, W_T=72um at Vgs=Vds=1.1V.

de-embedded and simulated value of Sid is observed (≈5% for 40nm NMOS device at 67GHz).

VII. Conclusion

67GHz noise measurement of 40nm technology device is presented for the first time. By employing statistical noise extraction technique and setup with improved noise receiver sensitivity, robust noise parameters data could be obtained even on highly mismatched 40nm CMOS device. The validity of the measurement data has been confirmed by its correlation with model and theoretical prediction

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