Advanced Non-linear Model for Accurate Prediction of Harmonically Terminated Power Amplifier Performance

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Abstract **— This paper presents recent advances in the state-of-the-art of Neural Network modeling of microwave FET devices. Enhanced accuracy of the Adaptive Knowledge-Based Neural Network (AKBNN) model is shown by comparing predicted load-pull performance of the device to measurements in an automated harmonic load-pull system. Test devices are a 1.2mm HFET measured at 2.2 GHz, and a 4.8mm pHEMT at 8.4 GHz. Modeled versus measured comparisons include power-added efficiency and output power under fundamental frequency and second and third harmonic frequency tuning. The effectiveness of this modeling approach for the design of high-efficiency power amplifiers operating in Class-E or Class-F modes is discussed.**

Index Terms **— Impedance measurement, neural network applications, modeling, microwave power FETs, power amplifiers.**

I. INTRODUCTION

Harmonic tuning is a well-known technique for improving the power-added efficiency (PAE) of power amplifiers. This is an important performance feature for some terrestrial applications where battery life needs to be extended, and for many space applications where prime spacecraft power is limited. It has been shown theoretically [1] and demonstrated experimentally [2] that significant improvement in power-added efficiency is possible by using the harmonic frequency components at the device drain to shape the drain voltage and current waveforms, thus keeping the instantaneous current-voltage product low. The practical implementation usually takes the form of a Class-F or Class-E amplifier and focuses on design of the correct load impedance at the fundamental and second and third harmonic frequencies for optimum PAE performance. The higher-order harmonics have progressively smaller impact on the overall performance and may lead to unnecessary complications in the output matching network.

The key to achieving cost-effective design of a high-efficiency power amplifier is to have a CAD compatible FET device model that maintains accuracy over a broad range of power levels and bias voltage conditions. Harmonic generation is necessary for proper waveform shaping at the drain, and the voltage levels at the harmonic frequencies must be accurately modeled as a function of load impedance as well as gate and drain bias. In addition, the drain-source current at the quiescent bias point (Class-A to Class-B) will have an impact on efficiency performance and is a useful parameter to examine during circuit optimization in the design phase. This requires that the device model maintain accuracy in gain compression up to saturation as well as gate biases from Class-A operation down to pinch-off. Device models based on closed-form equations have typically shown limitations in both of these regions, which compromises a full optimization of amplifier performance.

To overcome these limitations we have developed a new adaptable neural network FET (ANNFET) model that has the capability of being dynamically reconfigured by the user [3]. A detailed comparison is made between the model predictions under computer simulated harmonic load pull conditions, and the measurements obtained in an automated harmonic load pull system. The comparisons are performed at the device level, without the additional uncertainties introduced by a full amplifier circuit.

This CAD compatible Neural Network device model will contribute to power amplifier design technology in several areas. First, it will enable accurate optimization over operating regions where existing models have shown weaknesses. Second, it will reduce the time and expense of experimental load pull measurements as preliminary steps to power amplifier design. In addition, it will allow designers to explore the potential benefits of harmonic tuning on the gate side of the circuit without the hardware expense of including this feature in existing load pull setups. Finally, it may be applied to high-efficiency amplifier design at Ka-band and higher frequencies where

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experimental harmonic load pull measurements are not always feasible.

The organization of this paper is as follows. Section II gives a brief outline of how the ANNFET model was dynamically configured for the given application. Section III gives a description of the harmonic load pull system. Finally, Section IV will present a detailed comparison between the model predictions under computer simulated harmonic load pull conditions, and the measurements obtained in the automated harmonic load pull system. Results will include power-added efficiency and output power under fundamental frequency and second and third harmonic frequency tuning.

II. The Configuration of the ANNFET

A. The ANNFET Model

The ANNFET model used in this work was dynamically configured with Ids, Cgs and Cgd as nonlinear elements realized with Knowledge-Based Neural Networks (KBNNs) as shown in Fig. 1, while all the other elements were specified as static lumped linear elements. This network was implemented into Agilent's Advanced Design System (ADS), where we used the harmonic balance method (HBM) for steady-state analysis of nonlinear periodic circuits.

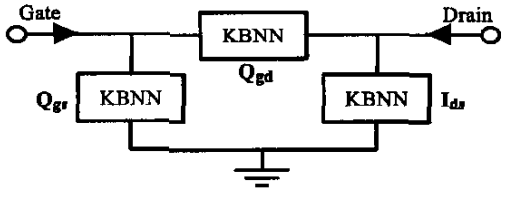

Fig. 1. Circuit representation of three output parameters at neural network output layer where $y=[Q_{gs}, I_{ds}, Q_{gd}]^T$. This network is used to supply currents and charges as its output in the HBM when given V_{ds} and V_{gs} as inputs.

B. The Knowledge-Based Neural Network (KBNN) Architecture and its Training.

The KBNN structure is known for its ability to utilize microwave information in the form of empirical functions or analytical approximations incorporated into the neural network. We also took advantage of the KBNN ability to extrapolate beyond measured data, which reduced the need for a large set of training data. The fundamentals of knowledge-based neural network (KBNN) structures have been developed in the literature [4]; as a result, we will briefly review the important aspects of the KBNN structure and the empirical functions incorporated into the knowledge layer as well as the boundary layer.

The KBNN structure used in this work is a seven-layered non-fully connected structure shown in Fig 2.

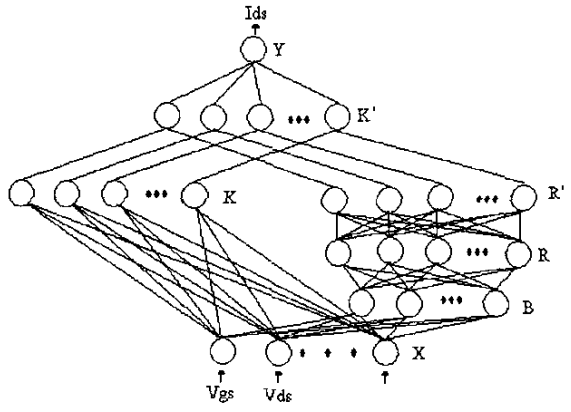

Fig. 2. The KBNN Structure.

The seven layers in the KBNN are referred to as an input layer X, a knowledge layer K, boundary layer B, region layer R, normalized region layer R', normalized knowledge layer K' and output layer Y. The Knowledge layer K consists of information in the form of empirical functions $\Psi(.)$,

$$k_i = \Psi_i(x,w_i), \qquad i = 1,2,\ldots,N_k \tag{1}$$

x is a vector of inputs x_i, $i = 1,2,\ldots,N_x$ and w_i is a vector of parameters in the empirical formula. In the case of drain current Ids, the following equation developed by I. Angelov [5] is used as the knowledge equation in the Knowledge layer;

$$\Psi = P_1(V_{gs} - V_{pk}) + P_2(V_{gs} - V_{pk})^2 + P_3(V_{gs} - V_{pk})^3 \tag{2}$$

$$I_{ds\,(Angelov)} = I_{ds} = I_{pk}(1+\tanh(\Psi))(1+\Lambda V_{ds})(\tanh(\alpha V_{ds})) \tag{3}$$

This equation can successfully model a typical family of IV curves, however, we needed to model IV curves well below pinch off. This work uses the Bayne equation [6] in conjunction with the Angelov equation.

$$I_{ds(Bayne)} = I_{ds} = I_{pk}(1+\beta(V_{gs}-Z)^2)(1+\Lambda V_{ds})(\exp(\Gamma V_{ds})-1) \tag{4}$$

This equation was combined with the Angelov expression for current in the Knowledge layer to produce a new expression capable of modeling a wider range of DC IV curves.

$$I_{ds} = (I_{ds(Angelov)})(1+\tanh(S_2 V_{gs} - M_2)) + (I_{ds(Bayne)}) \tag{5}$$

Note that when the equations are combined, the term $(1+\tanh(S_2V_{gs}-M_2))$ allows the network to switch between $(I_{ds(Angelov)})$ and $(I_{ds(Bayne)})$. There is a particular V_{gs} value that will cause the neural network to switch between one equation or the other. This switching mechanism is controlled by the neural network through adjustment of the parameters S_2 and M_2.

Knowledge equations were also needed for capacitance. Attempts were made to use the capacitance equations developed by Angelov, however, modifications were made to improve training of the network. The unique knowledge equation developed for gate-source capacitance is:

$$C_{gs(Bayne)} = C_o(1+\tanh(P_o+P_1(V_{gs} - \chi)))(1 +\tanh(P_2 +P_3V_{ds})) \quad (6)$$

The unique knowledge equation developed for gate-drain capacitance is:

$$C_{gd(Bayne)} = C_o(1+\tanh(P_o-P_1V_{ds}))(1+\tanh(P_2+P_3V_{gd}))(1+\tanh(P_4+P_5V_{gs})) \quad (7)$$

These capacitance expressions were chosen to account for charge conservation. In addition, transcapacitance is avoided by calculating each capacitance as a function of the voltage across its local terminals. The resulting model is ensured to be charge-controlled.

The boundary layer is represented by an arbitrary vector b that incorporates knowledge in the form of problem dependent boundary functions or, in the absence of boundary knowledge, as linear boundaries $B_i(x,v_i)$. The weights in the boundary layer are represented by the adjustable parameters or coefficients in the boundary equation, noted as v_i where v is a vector whose size is determined by the number of coefficients in the equation. Neuron i in this layer is calculated by

$$b_i=B_i(x, v_i), \quad \text{where } i=1\ldots N_b \quad (8)$$

The boundary equation used in this work for the current is the derivative of the current expression with respect to both V_{gs} and V_{ds}; $(\partial^2 I_{ds}/(\partial V_{gs}\partial V_{ds}))$. The associated boundary expression for the capacitance is the integral of the capacitance expression with respect to V_{gs}, given by $(\int C_{gs(Bayne)}\partial V_{gs}$. To train the KBNN we employed the Levenberg-Marquardt method to minimize the error function. The overall strength of this method is its general reliability in solving nonlinear least squares problems.

III. Harmonic Load Pull System

A block diagram of the automated harmonic load pull system is shown in Fig. 3. A frequency synthesizer is used to establish the RF input signal. For our test devices the system required a driver amplifier after the synthesizer to set the correct input power dynamic range.

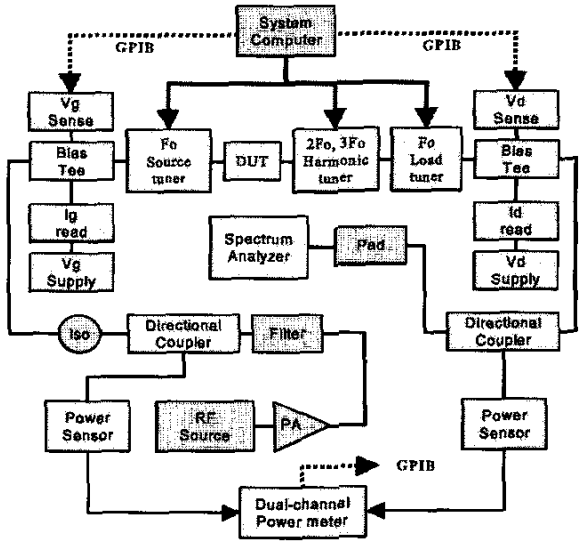

Fig. 3. The automated harmonic load pull system.

A low-pass filter is used to attenuate harmonic content from the driver before the signal enters the first directional coupler. A clean input signal is verified by an independent measurement with the spectrum analyzer.

The system uses precision tuners from FOCUS Microwaves, Inc., consisting of source and load fundamental tuners, and a load harmonic tuner. Supporting test equipment to provide bias and read gate/drain current levels and sense gate/drain voltages is connected to the computer through a GPIB interface. The spectrum analyzer is included to monitor signs of device instability during power and efficiency contour measurements.

IV. Modeled vs Measured Results

Fig. 4 summarizes the measured and modeled results for a 1.2mm HFET measured at 2.2 GHz, and a 4.8mm pHEMT at 8.4 GHz. The modeled results were derived from a computer simulation with the ANNFET model, using the source impedance determined by the load pull system. Computer optimization was done to find the load impedances for optimum power and efficiency performance, which converged to the same values as

determined experimentally from the load pull system. The MIC test substrate for the 4.8mm device included a gate partial matching structure to transform the low input impedance to a higher level for effective matching with the source tuner. The modeled results include the effect of this network, as well as the gate and drain bond wires.

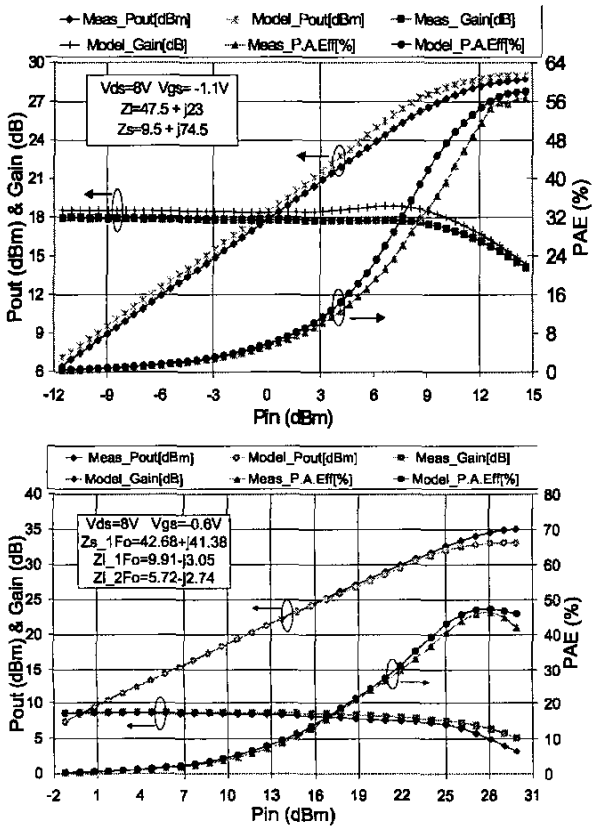

Fig. 4. Model simulation vs. measurement for output power, gain, power-added efficiency for 1.2mm HFET at 2.2 GHz (top), and 4.8mm pHEMT at 8.4 GHz (bottom).

The model was extended to the confirmation of experimental harmonic load pull results under Class A to Class A/B bias conditions. The device model was terminated with the experimentally determined optimum fundamental source and load impedances. The drain side was then terminated with the experimental optimum harmonic impedances as determined by harmonic phase sweep measurements. The measured vs modeled results for the 1.2mm and 4.8mm devices are shown in Table 1 for two representative bias conditions.

TABLE 1
Measured vs Modeled Harmonic Load Pull Results

Frequency=2.2 GHz, 1.2 mm HFET			
Bias	Parameter	Model	Measured
Vds=5V	PAE (peak)	72%	70%
Vgs=-1.2V	Pout @ PAE peak	24.3 dBm	24 dBm
Vds=7V	PAE (peak)	67%	65%
Vgs=-1.2V	Pout @ PAE peak	26.3 dBm	27 dBm
Frequency=8.4 GHz, 4.8 mm pHEMT			
Vds=8V	PAE (peak)	47.4%	46.3%
Vgs=-0.6V	Pout @ PAE peak	33dBm	34.5dBm
Vds=7V	PAE (peak)	49%	47.2%
Vgs=-0.4V	Pout @ PAE peak	32.6dBm	34.9dBm

V. Conclusions

This work has presented new techniques for the Neural Network modeling of FET devices. The method has been applied to HFET and pHEMT devices up to X-band, in Class A to Class A/B bias conditions, with harmonic tuning, and demonstrated that useful performance predictions can be made for the modeling and optimization of harmonically tuned power amplifiers.

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