1603 St-Regis
D.D.O., Quebec H9B 3H7, Canada
Tel 514-684-4554 Fax 514-684-8581
E-mail: info@ focus-microwaves.com
Website: http://www.focus-microwaves.com

Application Note 44

Nonlinear Transistor Testing using Highly Accurate Harmonic Load Pull Tuners[+]

Summary

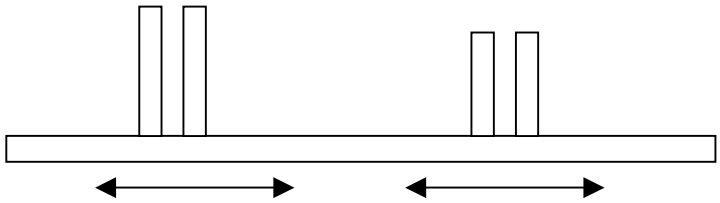
Highly reflective harmonic tuners with fine resolution tuning accuracy between 0.2° and 0.7° over the whole 0-360° tuning range have been developed and are used in nonlinear transistor testing. These tuners are used in a compact and accurate harmonic load pull system. The system allows characterizing complex and strongly nonlinear behavior of microwave transistors including: hot IV curves, saturation plots and load pull contours and 2nd and 3rd harmonic impedance pulling. The exceptional accuracy of the tuners is obtained through precise alignment supported by calibration and nonlinear interpolation algorithms; these allow reproduction of arbitrary impedances with accuracy typically exceeding -50dB, at the very edge of the Smith Chart.

Introduction

Stringent requirements in new wireless amplifier designs with respect to Power added Efficiency (PAE), Output Power and Linearity (IMD, TOI or ACPR), but also with respect to fast design-turnaround, made harmonic tuning, a couple of years ago still an exotic endeavor, to a standard test procedure. Among the three available techniques [1], 'active harmonic load pull', 'passive harmonic tuning using triplexers' and 'passive tuning using frequency selective harmonic tuners', the last method is the most popular one, because of its compactness, affordability, easy implementation and frequency adjustability, while delivering useful and accurate data. This technique uses Focus' proprietary designs of harmonic load and source pull tuners[+] that can be installed also as an extension to already operating load pull systems.

The Harmonic Tuners

The harmonic tuners [2] use the simple principle of sliding resonator circuits connected in parallel to a very low loss transmission line. Tuners usually employ two sets of two resonators to cover the two harmonic frequencies, 2fo and 3fo (figure 1).



As shown in figure 1, it is required to use a set of two resonators to handle one harmonic frequency, because this allows compensating the residual reflection created by a single harmonic resonator at the fundamental frequency (figure 3).

[+]*Patent pending*

Focus' harmonic tuners generate a very high reflection factor between 0.95 and 0.99 at both harmonic frequencies over a 360° phase tuning change. This performance is typical up to 2GHz but then insertion loss in the transmission line reduces the reflection factor to values around 0.92-0.95. The amplitude of the reflection factor cannot be modified, but all experimental and modeling evidence to date shows that this is not required to fully characterize and optimize the harmonic tuning conditions of power transistors.

A typical frequency response of harmonic tuners is shown in figure 3:

Figure 2: Harmonic tuner 0.8-7GHz and sets of resonators for different frequencies in this band.

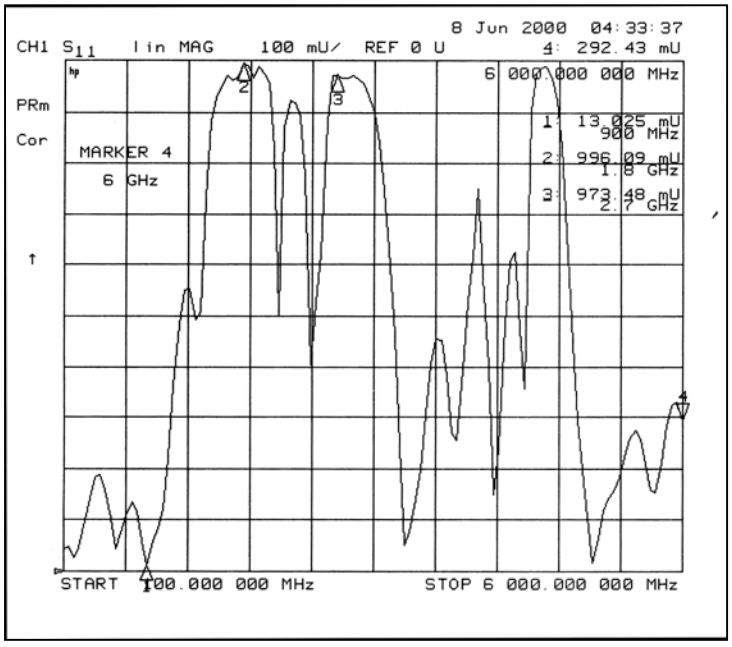


Figure 3: Typical response of harmonic tuners, tuned for fo=900MHz, 2fo=1.8GHz and 3fo=2.7GHz. The corresponding reflection factors read: S11(fo)=0.013 (marker 1), S11(2fo)=0.996, (marker 2) and S11(3fo)=0.973 (marker 3).

Calibration and Accuracy of Harmonic Tuners

The harmonic tuners are calibrated on an automatic network analyzer at both harmonic frequencies. For each position of the first set of resonators all user-defined impedances of the other harmonic are calibrated. After this, second order polynomial algorithms interpolate between calibrated points with very high accuracy and provide typical phase errors as low as 0.1°-0.6° and amplitude errors between -40 and -60dB (see figures 5,6).

Other software algorithms allow not only to compute and display the impedances associated with any arbitrary position of the resonators, but also to synthesize such impedances, i.e.: to physically move both resonators of the tuner to such positions as to generate the desired impedance.

The limit of the tuning resolution is given by the step size of the tuner motion mechanism, typically of the order of 12μm to 25μm, corresponding to minimum phase steps of 0.026° to 0.052° at 900MHz. The phase resolution obviously decreases inversely proportionate to the frequency. Tuners operating at higher frequencies (models up to 65GHz have been manufactured using the same concept) therefore use a lower step size, down to 3μm.

There are two quantities of interest in tuner performance,

- The mechanical repeatability expressed in RF quantities, like S11 and S21, between repeated settings of the tuner motors and
- The tuning accuracy of the tuner, which is more important for RF testing. This accuracy is defined as the vector difference between any tuned impedance and the actual value measured by the network analyzer. Focus systematically verifies the performance of all its tuners using the 'tuning accuracy' method.

For testing the 'tuning accuracy' harmonic tuners are calibrated at a number of points (typically 20x20=400 or 40x40=1600 points). The first number is the points for 2fo and the second number the points for 3fo (figure 4). Then a special routine is executed, which sweeps the phase of S11 (2fo) and S11 (3fo) in equal phase steps between 0° and 360°, with step sizes varying between 1° and 10°. It is to be noticed that these points are not calibrated points; instead they are interpolated points, because even at the highest calibration density the distance between calibrated points is at least 9° (360°/40). Tuning accuracy data of such tuners are shown in figures 5 and 6.

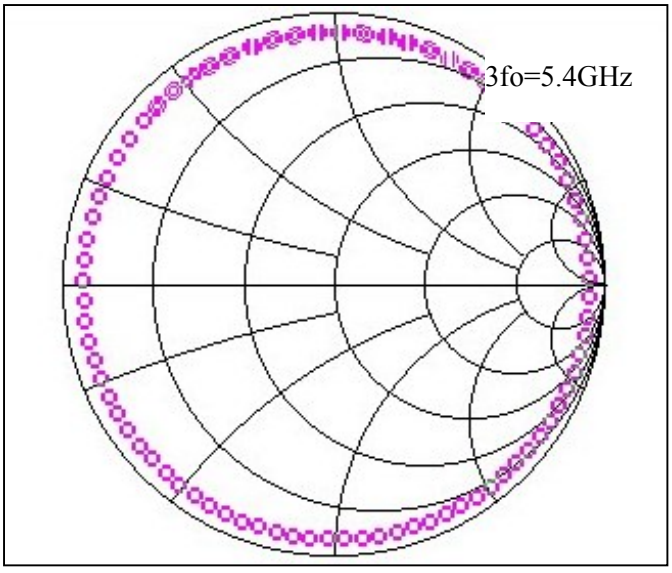


Figure 4: Calibration pattern of harmonic tuners at 1.9GHz. Shown points are for 3fo. The 2fo pattern includes even higher Γ. Phase step between calibrated points is 9°. This plot shows overlapping sweeps.

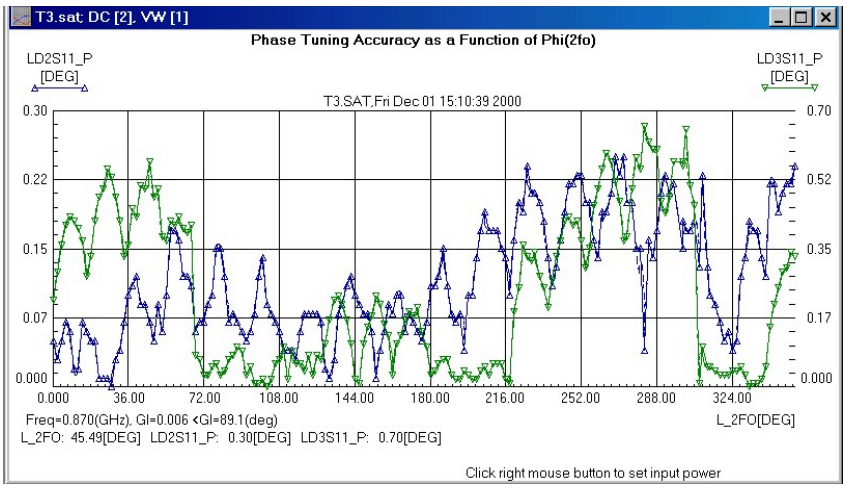


Figure 5: Tuning accuracy of harmonic tuner at 870MHz;
Tuning Phi(2fo):
Maximum error:
at 2fo= 0.23°
at 3fo= 0.65°.
Calibration phase step= 9°, measurement phase step= 2°.

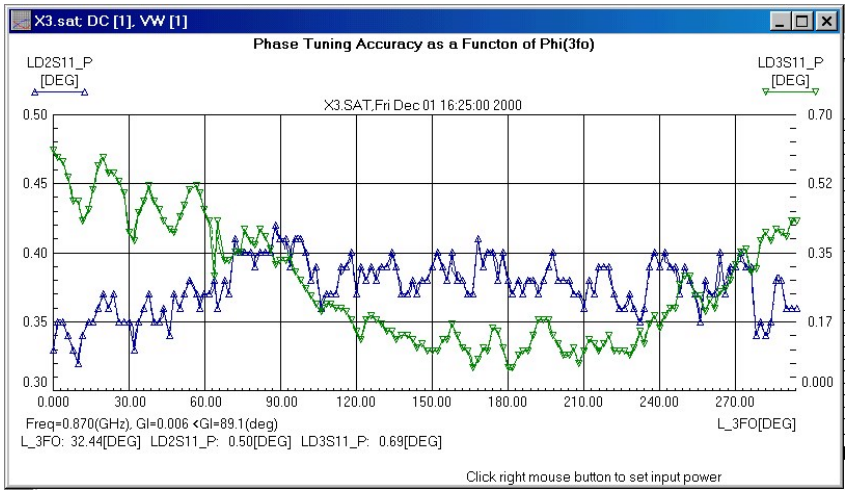


Figure 6: Tuning accuracy of harmonic tuner at 870MHz;
Tuning Phi(3fo):
Maximum error:
at 2fo= 0.40°
at 3fo= 0.65°.
Calibration phase step= 9°, measurement phase step= 2°.

Harmonic Load Pull Setup

A compact harmonic load pull setup is used to test power transistors. It includes one or two harmonic tuners (for source and/or load) and two fundamental tuners, in general with a prematching configuration for very high VSWR (up to 150:1). A desktop PC controls all components of the setup and associated GPIB instruments.

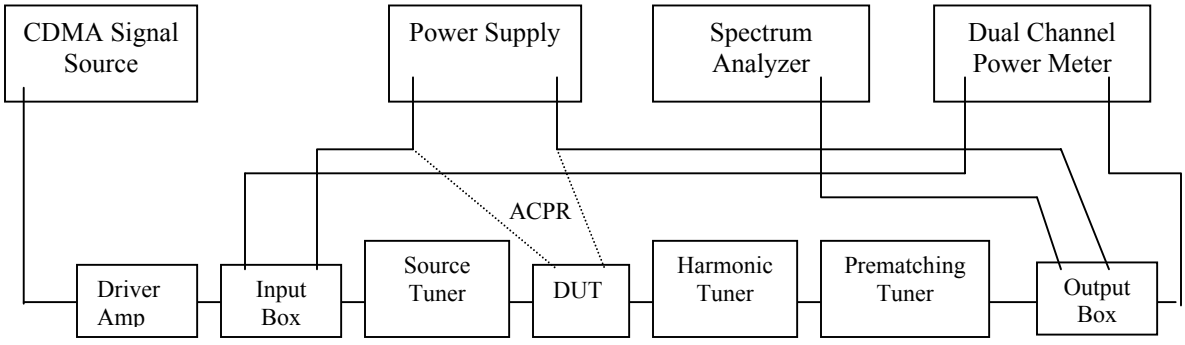


Figure 7: Block diagram of harmonic load pull setup.

The setup includes a synthesizer source and, alternatively, a CDMA source, a linear power driver amplifier; an Input Box including an isolator, directional coupler and bias tee, a programmable power supply, spectrum analyzer and dual channel power meter; it also includes a fundamental source tuner, model CCMT-1808, 0.8-18GHz, (a harmonic tuner is supported by the control hardware and software and can be added at any time) and a DUT in a microstrip test fixture (model PTJ-0); at the output there is a harmonic tuner, model PHT-1816, 1.6-18GHz, and a prematching tuner, model PMT-1816, 1.6-18GHz. The Output Box includes a bias tee, a 30dB attenuator and a directional coupler to connect to the spectrum analyzer. The tuners can operate to 18GHz, but some passive components limit this to around 6-7GHz.

The CDMA source allows ACPR measurements. If ACPR is measured then the bias tees in the input and output box cannot be used, because down-and up-converted modulation components of the CDMA signal, enhanced by series resistances and inductances in the long bias lines (through the test fixture and the tuners), will deteriorate the accuracy of the measurement. In this case (for ACPR measurements) the bias lines through the input and output boxes shall be replaced by bias networks manufactured directly on the test fixture.

An actual photograph of the setup in Focus' training room is shown in figure 8.

Figure 8: Harmonic load pull setup using load prematching tuner

The harmonic load pull software (figure 9) allows testing most nonlinear characteristics of the transistors under fully controlled source and load impedance conditions at all three harmonic frequencies. Testing of all RF and DC quantities as a function of frequency, input power, DC bias and fundamental and harmonic impedances are standard features. A complete MACRO language allows automating most test procedures.

Further data processing routines, like 'DesignWindow' allow easy search through cumbersome load pull files to find optimum conditions for combined requirements, like PAE, Pout and ACPR, which would, otherwise require complex graphical multi-contour overlapping.

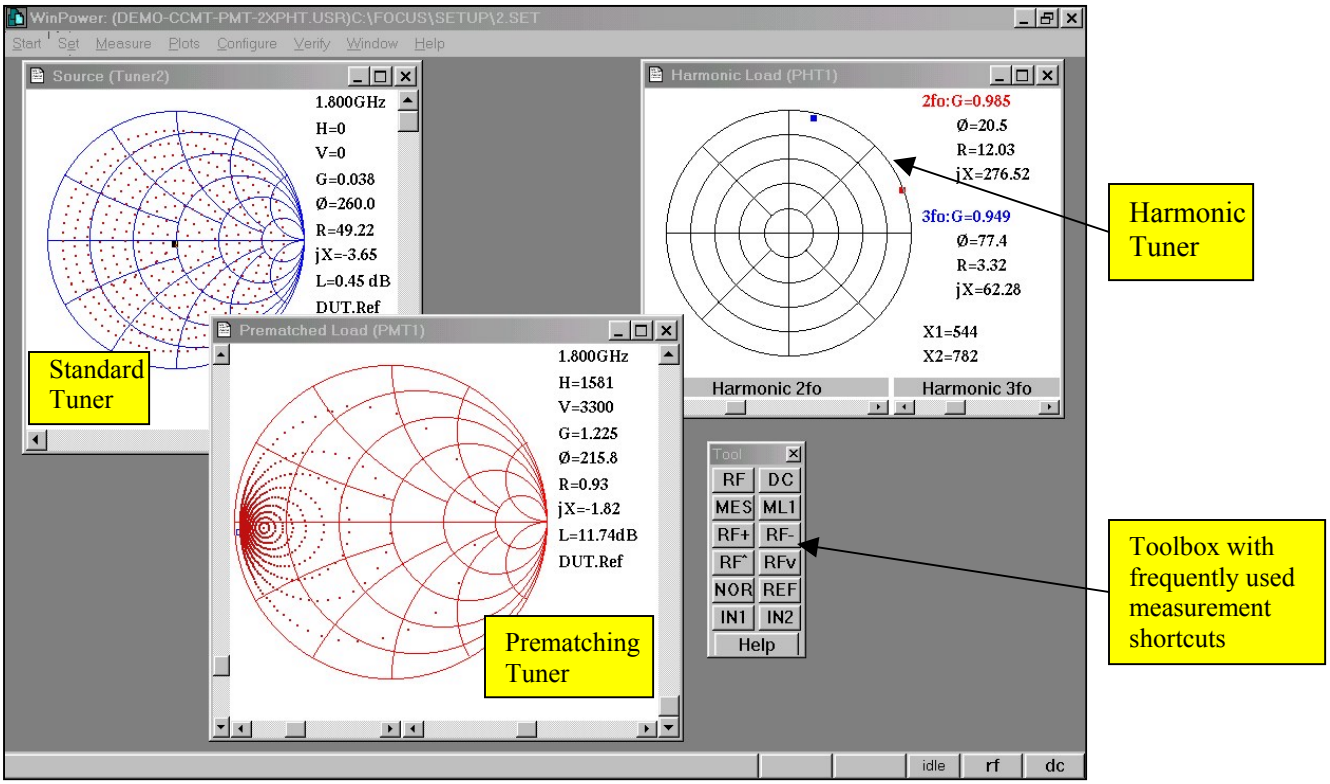


Figure 9: Harmonic Load Pull software, showing calibration points of the source and load tuner and a set of impedances generated by the output harmonic tuner at 2fo and 3fo.

Nonlinear DC, RF and Harmonic Testing

Power transistors can be tested using the described setup in regard to Output Power, Power Added Efficiency (PAE), Gain, Adjacent Channel Power (ACPR), Intermod (second and higher order), Third Order Intercept (TOI) and many other RF quantities. At the same time IV characteristics can be measured under 'cold' (Pin=0) or 'hot' (Pin > 0) conditions. During these tests all associated Impedance parameters at the transistor ports and all three harmonic frequencies can be controlled and documented [3].

Ordinary load pull consists in sweeping all or part of the Smith Chart with the fundamental load or source impedance, whereas Harmonic load (source) pull consists in sweeping all phases between 0° and 360° of the second (2fo) and third (3fo) harmonic impedance. Ordinary load pull contours are well known from the literature and for this reason this note does not include any.

Automatic Peak Search routines allow determining the optimum impedances at any of the three frequencies. These search routines are not limited to calibrated points but use any interpolated point and high-resolution impedance synthesis algorithms.

Figure 10 shows the effect of harmonic loads on 'hot' IV curves of a FET. 'Hot' means that the IV characteristics have been measured as the transistor is injected nominal RF power adjusted to drive the device into 1dB gain compression (P1dB). The left plot shows IV curves under the following load conditions:

Source and load are power matched at the fundamental frequency fo (1.7GHz); Zs(2fo)= ZL(2fo) = 0 (Short circuit); Zs(3fo) = ZL(3fo) = ∞ (Open circuit). The right plot shows the IV curves again under matched conditions for fo but: Zs(2fo)= ZL(2fo) = ∞; Zs(3fo) =ZL(3fo) = 0;
We observe a considerable variation of the drain current by a factor of nearly 2, just by swapping the harmonic loads from Open to Short.

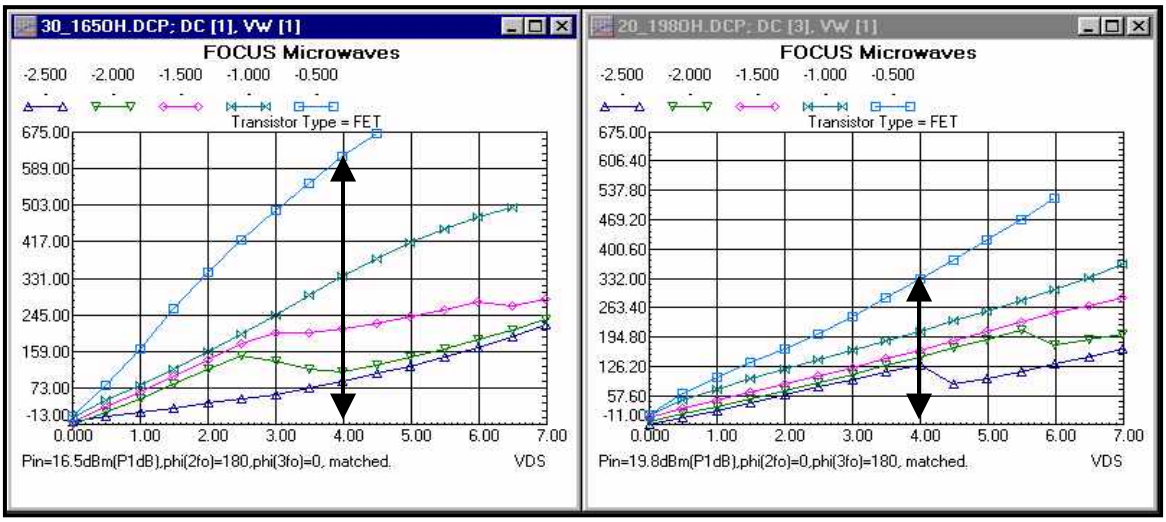


Figure 10: Effect of harmonic loading on 'hot' IV curves of a medium power FET. Pin is selected for P1dB compression in both cases.

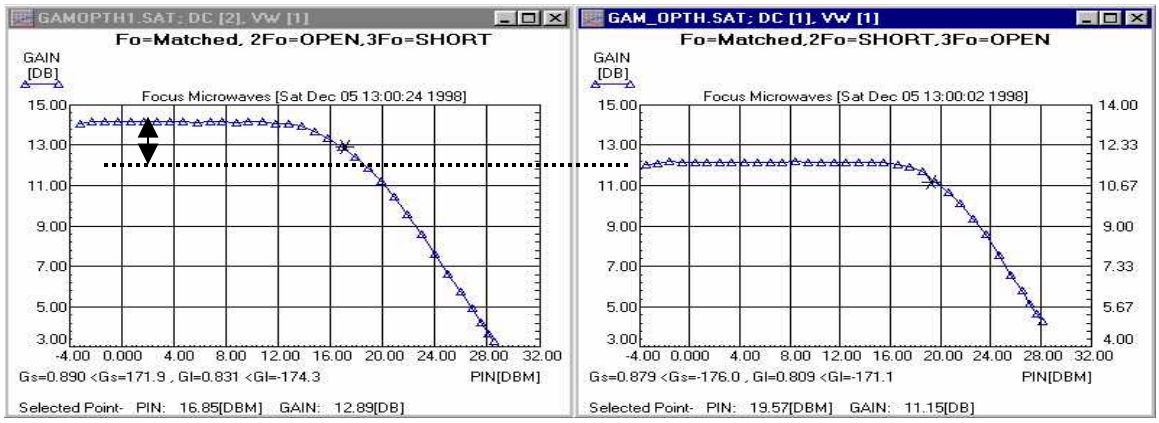


Figure 11: Effect of harmonic loading on Power saturation plots of a FET. Left: Z(2fo)=Open; Z(3fo)=Short; Right: Z(2fo)=Short, Z(3fo)=Open. In both cases the fundamental impedances are set for maximum gain/output power conditions.

In figure 11 the effect of harmonic loading is obvious, in particular in what concerns the 1dB gain compression point. On the left side we have P1dB = Pin+Gain = 16.85 + 12.89 = 29.74 dBm; on the right side we have P1dB = 19.57 + 11.15 = 30.72 dBm, or an increase by 1dB; as can be seen from figure 12, an increase in output power of 1dB typically corresponds to an increase in PAE of more than 25% for the same compression (=linearity).

Finally more nonlinear (harmonic) test results on harmonic phase sweeping are presented in figure 12. The software routine that accomplishes these tests allows the user to select

an arbitrary starting phase and any phase step, from coarse values of 10° down to fine steps of less than 1°. The tests shown here use a step of 5°. Again these are interpolated and not calibrated points.

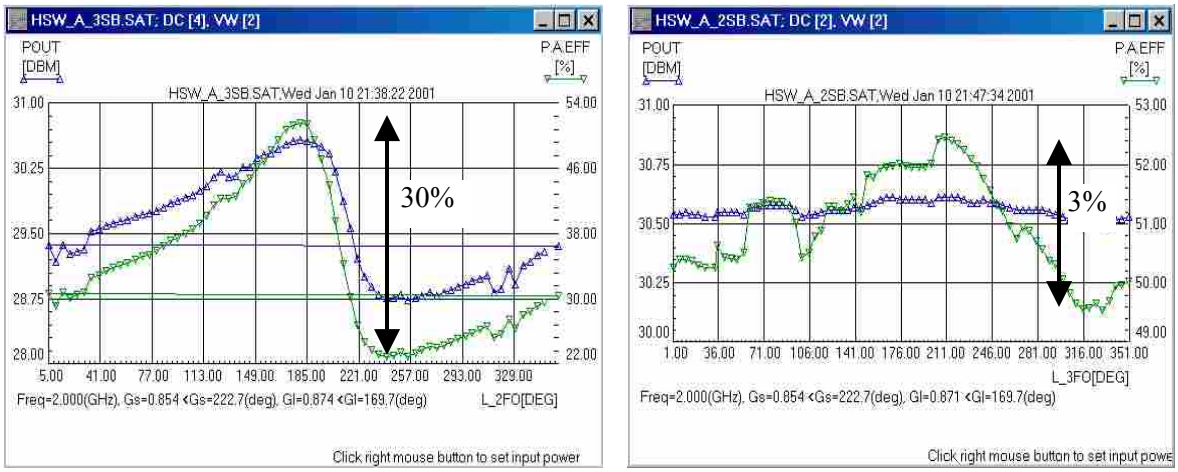


Figure 12: Effect of second (left) and third (right) harmonic phase tuning on PAE and Pout Fundamental frequency = 2.0 GHz.

Figure 12 shows the effect of second and third harmonic phase tuning on Power Added Efficiency (PAE) and Output Power. Tuning of 2fo increases PAE by close to 30% whereas tuning of 3fo has an effect of about 3%. These tests have been carried through under 'class A' operation, with Id ≈ 0.5 Idss. Similar tests made under class F operation (Id ≈ 0) show similar changes in PAE for 2fo tuning but the changes for 3fo tuning are typically 3 times higher (9%), for the same device and the same drain bias.

References

[1] "Brief Comparison of Harmonic Load Pull Systems", Technical Note 1-2000, Focus Microwaves, Inc. February 2000.

[2] "Programmable Harmonic Tuner, PHT", Product Note 44, Focus Microwaves, Inc., November 1997.

[3] "Nonlinear Characterization of Power Transistors", Focus Microwaves Presentation at Wireless Conference 2001, San Jose, California, February 2001.